High-speed hybrid III-V-ON-SI vertical cavity lasers

Topic, Vladimir

Publication date:
2019

Document Version
Publisher's PDF, also known as Version of record

HIGH-SPEED HYBRID III-V-ON-SI VERTICAL CAVITY LASERS

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A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

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February 2019

Project period:	March 2015 - February 2019
Project funding:	Innovation Fund Denmark HOT project (Grant No. 5106-00013B)
Main supervisor:	Associate Professor Il-Sug Chung
Co-supervisor:	Dr. Luisa Ottaviano
Ph.D. defense date:	28^{th} May 2019
Ph.D. defense committee:	• Associate Professor Kresten Yvind, Technical University of Denmark, Denmark • Dr. Dan Birkedal, Alight Technologies, Denmark • Ingénieur chercheur Badhise Ben Bakir, CEA-Leti, France

Abstract

Vertical cavity lasers (VCLs) are the dominating laser type for the short-reach fiber optical links, with rising interest in employing them across the wider range of optical interconnects. From micrometer length links in silicon (Si) photonics to long distance fiber links in mega data centers, the VCLs lasing at long wavelengths could satisfy the rising requirements for the high power efficiency and modulation speed.

A novel design of hybrid III-V-on-Si VCLs is investigated in this thesis. It employs a high-index-contrast grating (HCG) as one mirror and dielectric distributed Bragg reflector (DBR) as second mirror to achieve very compact optical mode volume which results in potentially ultra-high intrinsic bandwidth. The aim of this work is the experimental demonstration of the electrically pumped VCLs based on this design.

The first part of this thesis deals with the design of the proposed lasers. The theoretical background of the HCG is given, focusing on its application as a compact broadband reflector. Basic theory of the dynamic properties of the laser and the optimization of the design for the high modulation speeds is explained. The key features of the electrically pumped design are discussed, focusing on minimizing the parasitic elements. The methods of achieving current confinement, using proton implantation and selective undercut etching, are investigated. The low-resistance ohmic contacts are optimized to avoid deep metal diffusion.

The complete fabrication of proposed laser design is discussed and presented in the second part of the thesis. The wafer bonding for integrating III-V layers onto a SOI wafer has been one of the main fabrication challenges. To solve it, the adhesive bonding method using ultra-thin polymer layers has been successfully implemented and optimized. The complete fabrication procedure for the hybrid VCLs has been developed using CMOS-compatible processes.

In the third part, the fabrication and characterization of several versions of VCLs is presented. Considerable efforts have been put in to demonstrate lasing; however, due to numerous fabrication obstacles this was not achieved. The first fabricated lasers showed no light emission due to issues with the epitaxy design. The poor wafer quality of the second epitaxy caused deviations during fabrication and low yield. The final fabricated design showed better properties, although the lasing was not reached due to too high threshold. The results of the experimental work are discussed focusing on prospects of optimizing the device design and fabrication to achieve successful demonstration of high-speed lasers.

Resumé

Vertikale kavitetslasere (VKL) er den dominerende laser type når det kommer til kort-rækkevidde optiske forbindelser, med stigende interesse i anvendelse til en bred række af optiske forbindelseselementer. Fra mikrometerskala i silicium (Si) fotonik til fiberkoblinger over lange afstande i mega data centre, kan VKL lasere ved en lang bølgelængde indfri de stigende krav til høj ydeevne og modulationshastighed.

Et nyt design af hybrid III-V-på-Si VKL undersøges i denne afhandling. Den anvender et højt indekskontrast gitter (HKG) som det ene spejl og en dielektrisk distribueret Bragg reflektor (DBR) som det andet spejl til at opnå en meget kompakt optisk mode-volumen der resulterer i en potentiel ultra høj intrinsisk båndbredde. Målet for dette arbejde er at eksperimentelt demonstrere en elektrisk pumpet VKL baseret på dette design.

Den første del af afhandling gennemgår designet af foreslåede lasere. Den teoretiske baggrund for HKG gives, med fokus på dens anvendelse som en bredbåndsreflektor. Basal teori omkring de dynamiske egenskaber af lasere præsenteres og optimeringen af design for at opnå høj modulationshastighed gennemgås. Nøgleegenskaberne af et elektrisk pumpet design diskuteres med fokus på a minimere parasitære elementer. Metoderne til opnåelse af ladningsbærerindespærring ved brug af fotonimplantation og selektiv underskåret ætsning undersøges. De ohmiske kontakter med lav modstand optimeres for at undgå en dyb diffusion af metal.

Hele fabrikationsprocessen af det foreslåede laser design præsenteres og diskuteres i afhandlingens anden del. Waferbinding for at integrere III-V lag på en SOI wafer har været en af hovedudfordringerne i fabrikationen. For at løse denne udfordring er en klæbende bindingsmetode med brug af ultra tynde polymer lag blevet implementeret of optimeret. Hele fabrikationsprocessen for hybrid VKL er udviklet med CMOS kompatible processer.

I tredje del præsenteres fabrikationen og karakteriseringen af adskillige versioner af VKL. Betydelige bestræbelser har gået til at demonstrere lasing. Dette er imidlertid ikke opnået på grund af talrige fabrikationshindringer. De første fremstillede lasere viste ingen lysemission pga. problemer med epitaxidesignet. Den lave waferkvalitet ved den anden epitaxi medførte variationer underfabrikation og et lavt udbytte. Det endelige fabrikationsdesign viste bedre egenskaber men lasing ikke blev opnået på grund af en for højt tærskel. Resultaterne af det eksperimentelle arbejde diskuteres med fokus på udsigterne til at optimere enhedsdesignet og fabrikationen så højhastighedslasere succesfuldt kan demonstreres.

Preface

This thesis is submitted to the Department of Photonics Engineering at Technical University of Denmark (DTU) for the partial fulfillment of the requirements for the degree of Doctor of Philosophy (Ph.D.). The work presented here is part of the Ph.D. project which was carried out in the Quantum and Laser Photonics group from March 15th, 2015 to February 14th 2019. The project has been supervised by main supervisor Assoc. Prof. Il-Sug Chung, and co-supervisor Dr. Luisa Ottaviano.

The Ph.D. project was mainly financed by the Department of Photonics Engineering at Technical University of Denmark (DTU) and Innovation Fund Denmark through the HOT project (Grant No. 5106-00013B).

Acknowledgements

First and foremost, I would like to thank my supervisor Il-Sug Chung for giving me the opportunity to work on such an exciting and challenging project. I am grateful for his guidance, support, endless patience and inspiring perseverance. I would like to thank also my co-supervisor Luisa Ottaviano for sharing her expertise in cleanroom fabrication, as well as her understanding, support and friendship during difficult times.

A special thanks to Gyeong Cheol Park for being my unofficial mentor in cleanroom and for sharing his experience in characterization. Also, I am thankful to my teammate Sushil Tandukar, who worked side by side with me, for sharing all the ideas and experiences. Their involvement has been invaluable, and I wish to acknowledge their contribution in development of many fabrication processes used in this work. To Alireza Taghizadeh I thank for the discussions and sharing his knowledge on the theory behind this work. I would like to thank Kresten Yvind for helping me with characterization setup and for sharing his experience on laser physics and characterization.

Furthermore, I wish to thank all my colleagues in Quantum and Laser Photonics group and Nanophotonic Devices group for creating a fruitful and collaborative working atmosphere, all the constructive feedback, knowledge sharing and discussions, both inside and outside the cleanroom. Special thanks to Kristoffer Skaftved Mathiesen for help with the Danish translation of the abstract for this work. Additionally, I would also like to thank DTU Danchip staff for their expertise, help and support in the cleanroom.

I wish to acknowledge the Innovation Fund Denmark for funding the Ph.D. project, and the Otto Mønsteds Fond for economical support towards conference participation.

I will be forever grateful to my dear friends for always believing in me, pushing me further and being greatest inspiration in my life. A special thanks to my girlfriend for all the love, patience and encouragement in this difficult period. Last but not least, my deepest gratitude goes to my family for their continued encouragement throughout my life and for being there for me with unconditional love and support.

Vladimir Topić
DTU, Kongens Lyngby
February 2019

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CHAPTER 1

Introduction

In the recent years, data has become the most valuable resource in the world and the information is available to everybody all over the world. This has led to entire modern world's economy being based on information technology (IT). The top five largest companies in the world by market value by 2018 are all from IT sector, offering hardware and software that are now part of our everyday life, giving us access to all the information and enabling us to stay connected. Internet, online shopping, social networks, media streaming, cloud computing and storage are just a few examples of the services in use today that have caused the amount of data being transferred globally to increase by an exponential trend over the past few decades. New services, like the artificial intelligence, augmented reality and Internet of Things (IoT), that are already starting to spread, will push this trend even further in coming years. And the technology that enabled this kind of growth and, in a way, shaped the modern world is optical communications.

Development of the semiconductor diode lasers and the optical fibers were the milestones in communication technology that enabled us to use photons to transfer information across huge distances with high speed and low power consumption [1, 2]. Decades later, single frequency lasers, fiber optics, fast detectors, high frequency modulation, wavelength multiplexing, higher order modulation formats, etc. are used to carry petabytes of information from continent to continent. This technology was first employed to connect the continents, countries and cities and form long-haul global area networks (GANs) and wide area networks (WANs). Naturally, not long after, optical communication moved from long-haul backbones to the metropolitan area networks (MANs) and even local area networks (LANs), with fiber replacing copper cables at shorter and shorter distances [2]. Past decade has seen the need for optical communication technologies to be employed at even shorter distances between different parts of large electronic systems. Today, rack-to-rack (1 m to 100 m) and even board-to-board (50 cm to 100 cm) interconnects are commonly optical [3, 4]. In recent years, efforts have been focused on bringing optics to even shorter distances for chip-to-chip (1 cm to 50 cm) and even on-chip (100 μm to 1 cm) interconnects, but electrical interconnects still dominate all short-distance communications, especially on integrated circuit chips and on circuit boards [5].

1.1 Optical interconnects

1.1.1 Motivation

The unrelenting growth of data traffic has led to equally dramatic growth of data centers. Energy consumption of the biggest data centers today is comparable to a city of million people and in total, they eat up more than 3% if world's electricity, with projections that it could increase to 20% by 2025 [6]. The need to improve energy efficiency and reduce carbon footprint of data centers is obvious. With power usage effectiveness of modern data centers approaching close to theoretically perfect value [7], any future improvements will be minor and incremental. Therefore, further drastic improvement would have to come by improving the computing efficiency.

1.1.2 Limits of electrical interconnects

The drive to replace electrical interconnects is due to their fundamental physical limitations which pose a challenge for them to cope with the exponentially growing data traffic [5, 8]. For a long time, the strategy for improving the computing power was to increase the performance of a single computing unit. When the limits were reached, the strategy moved to increasing the number of the computing units, but then the efficiency and performance of the communication between computing units becomes a key factor that determines the performance of an entire computer system. In other words, now performance is dominated by the interconnection medium between chips rather than the devices at either end [9]. Apart from the limited bandwidth that can be reached, the biggest limitation of electrical interconnects is the energy consumption. Radio-frequency waves of electrical interconnects are guided using metal waveguides and wires. The increasing resistive loss in metals at high oscillation frequency dominates the propagation loss in electrical interconnects which limits their length and the density [3, 5]. The energy required for charging and discharging of electrical connections leads to losses in interconnects so significant that they account to as much as half of the total power consumption in computer units [3]. Furthermore, at high speed and density, the interconnects have issue with cross-talk and electromagnetic interference (EMI) through capacitive and inductive coupling [3].

1.1.3 Potential of optical interconnects

Optics has potential to improve on all of these issues. Optical interconnects can offer much greater bandwidth, lower power consumption, and decrease interconnect delays [2]. Light is guided using dielectric waveguides that have very low loss, so an optical interconnect can be employed where long distance is the limiting factor for electrical interconnects. Interconnect density can be increased drastically considering that optical fibers and waveguides have much smaller dimensions and do not suffer from EMI and signal cross-talk. The density can be further multiplied by employing wavelength division multiplexing (WDM). This density benefit was the main driver for the introduction of optical interconnects at shorter distances [5]. However, as discussed above, energy consumption is becoming more and more critical issue, especially as the distance decreases, and total energy per bit of the link becomes the leading criterion. Optics can potentially be more energy efficient since it doesn't need to charge the line to operating voltage [3], but it is limited by the efficiency of transmitter and receiver.

In order for optical interconnects to become a viable alternative for future use at the shortest distances they need to meet some very strict energy targets [10]. The single most energy demanding part of the optical link is the device that converts the electrical signal to the optical one. Optical output device with sufficiently low energy per bit is the single largest technological challenge for realization chip-to-chip and on-chip optical interconnects. Semiconductor diode lasers have been the main optical output devices used in communications for a long time. However, as distances become shorter, the density of interconnects and the number of the transmission lines grows, which means that the fabrication costs of a single laser becomes a big factor in the total costs. Despite their potential, optical interconnects will replace electrical interconnects only when they have higher performance at lower cost and strong manufacturability in high volume.

Long distance optical links employ edge-emitting lasers at wavelengths around 1550 and 1310 nm, at which respectively minimum of absorption and dispersion in the optical fibers occur. However, these devices cannot meet the targeted low energy consumption, low cost and small footprint that are needed for short distance optical interconnects. Instead, the most used laser type in optical interconnects are vertical-cavity surface-emitting lasers (VCSELs). They can have many features that make them attractive, such as higher energy efficiency, high-speed modulation, single longitudinal mode operation, low fabrication cost, narrow circular beam for convenient fiber coupling, small footprint, possibility of forming two-dimensional arrays, wafer level testing, etc. [11]. VCSELs, operating in the short-wavelength spectral range ($\lambda \sim 800 - 1000$ nm), and multi-mode fiber (MMF) links are dominating the short-reach optical interconnects used in data centers and high-performance computing systems where links are shorter than 300 m in most cases. However,

as the new data rate standards increase from 10 Gb/s towards 100 Gb/s, modal and chromatic dispersion in the MMF reduces the reach from 300 m to only 100 m [12]. On the other hand, the data centers are growing in size. Newer mega data centers can span across huge areas and multiple buildings with links reaching kilometers in length, beyond the reach of short-wavelength VCSELs and MMFs. There is much interest in bringing the low cost and high energy efficiency of the VCSELs to longer wavelengths for high-speed links of over several kilometers with single-mode fibers (SMFs), not only for data centers and LANs but even for MANs and WANs [11, 13].

Short-wavelength VCSELs (SW-VCSELs) in use today, typically emitting around 850, 980, and 1100 nm, are based on well matured gallium arsenide (GaAs) technology, with oxide apertures for electrical and optical confinement, developed during the 1990s [14–16]. Long-wavelength VCSELs (LW-VCSELs), based on indium phosphide (InP) and emitting around 1310 and 1550 nm, have been much bigger challenge. Suffering from less mature fabrication technology, problems related to material quality and fundamental issues with device design, they could not keep up with SW-VCSELs [13]. For longer wavelengths energy bandgaps in active region are smaller, which leads to more dominant Auger non-radiative recombination, lowering the gain and causing poorer temperature performance. Main issue of InP-based VCSELs is realization of epitaxial distributed Bragg reflectors (DBRs) with high thermal conductivity, high reflectivity, and high electrical conductivity [17]. Typically used lattice-matched InGaAsP/InP epitaxial DBR has low refractive-index contrast ($\Delta n \approx 0.2 - 0.3$), which means that large number of quarter-wavelength layers is needed for high reflection. Such thick mirrors have poor thermal conductivity, limiting the continuous-wave (CW) operation at high temperatures [18]. Only recently have the LW-VCSELs seen novel approaches that enabled significant progress in performance and commercialization.

1.1.4 Silicon photonics

In recent years, silicon (Si) photonics technology has started to attract a lot of interest for applications in optical interconnects. It still faces many issues [19], but it offers a lot of potential, and it is projected that Si photonics will be the fastest growing and the highest volume market segment for optical link in the next decade [2]. It benefits from using mature fabrication infrastructure of silicon microelectronics, which means that component price could be significantly lowered. State-of-the-art complementary metal-oxide-semiconductor (CMOS) technology is sufficiently advanced to fabricate virtually all Si photonic components [20]. Si photonics is inherently single-mode so it benefits from increased use of SMFs in mega data centers where it finds application for the switch-to-switch, long-range and high-speed links as well as for large channel counts and coarse wavelength division multiplexing (CWDM) application [12].

Silicon photonics seems to be the way to go for realizing chip-level optical interconnects [21]. Direct integration with silicon seems to be essential for minimizing system energy per bit, very high density and very low cost per connection [10]. Two approaches for the light sources for on-chip interconnects can be considered: an integrated optical modulator with an off-chip light source or direct-modulation of an on-chip light source. While the off-chip light source can be very efficient and temperature stable, it has disadvantages of relatively large coupling losses between the off-chip light source and the Si chip and a high packaging expense [21]. Truly on-chip optical interconnects would ideally have on-chip directly modulated source that could be fabricated using CMOS-compatible processes and integrated together with electronics [21, 22]. However, realization of good enough light source on silicon remains a challenge.

1.2 Lasers for silicon photonics

The challenge of making light source in silicon comes from fundamental property of its energy band structure. As illustrated in Fig. 1.1, in order to have efficient stimulated emission, direct band gap is necessary (like in some III–V compound semiconductors, GaAs and InP for example). However, Si is indirect band gap material and for radiative recombination to happen a third particle (phonon) must be involved, a process which has much slower rate. On the other hand,

non-radiative transitions like the Auger recombination and free-carrier absorption have faster rate, leading to very poor internal quantum efficiency of light emission in Si [20].

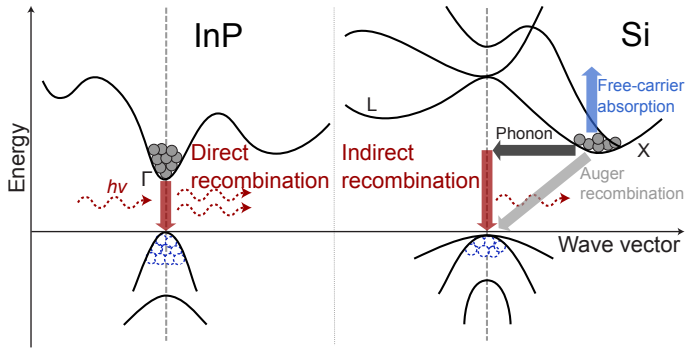


Figure 1.1: Simplified energy band diagrams of direct (InP, left) and indirect (Si, right) semiconductor showing the major carrier recombination processes. Optical transition requires conservation of energy and momentum, which is possible with direct bandgap. With indirect bandgap the dominating transitions are indirect via phonon, free-carrier absorption and Auger recombination.

Extensive research was done in effort to overcome this disadvantage of Si. Several different approaches resulted in successful light emission. Some of all-Si approaches like porous Si [23], Si nanocrystals [24, 25], Si Raman lasers [26], etc. are optically-pumped devices and therefore unsuitable for optical interconnect application. More promising approaches try to integrate another material onto Si platform to provide gain. These include doping with rare-earth ions like erbium (Er), hetero-epitaxial growth and hybrid approaches via bonding [20, 27].

Er-related devices are realized by doping Si-rich Si dioxide [28] or Si nitride [29], and while they show excellent gain under optical-pumping, due to the dielectric property of the material, high threshold voltages are required for electrical pumping. Challenge of achieving efficient electrical pumping makes Er-based Si lasers unlikely candidate for on-chip interconnect application.

Hetero-epitaxial Si lasers

Hetero-epitaxial growth of different materials on Si substrate can be separated into two directions: growth of germanium-based materials and growth of III-V materials. germanium (Ge) is also indirect band gap material but can be engineered to become direct by using n-type doping and tensile strain that comes from thermal expansion coefficient mismatch between Ge and Si [30] or using germanium-tin (GeSn) alloy [31]. Even electrically pumped laser has been demonstrated [32], however it still suffered from high threshold and poor emission efficiency.

Growth of III-V direct band gap material like GaAs or InP is very challenging due to large mismatches of lattice constants (4.1% and 8.1%, respectively) and thermal expansion coefficients (120.4% and 76.9%, respectively) compared to Si. This causes large amount of threading dislocations (TDs) which propagate to active layers and become non-radiative recombination centers, degrading the optical properties of such grown layers. Methods to avoid this problem are being researched and lasers have been demonstrated. A way to reduce TDs is to grow a thick buffer layers of SiGe [33], GaAs [34] or GaSb [35]. Also, nano-structures like quantum dots (QDs) help suppress TDs significantly. InAs/GaAs QD lasers have been demonstrated recently [36]. Challenging fabrication and reliability remains to be main issue with this kind of lasers.

Flip-chip bonded hybrid lasers

Hybrid integration via bonding can be achieved in two ways: direct mounting via flip-chip bonding or wafer bonding. In the first approach, III-V lasers diodes are fully fabricated and then such chip is flipped and attached to silicon-on-insulator (SOI) platform using solder bumps [37]. While

flip-chip integration allows for pre-testing and maintains excellent performance of lasers, it is a slow process and requires very accurate alignment to achieve good coupling of light from III-V to SOI. Assembly becomes costly process and complicated for mass production. It is not CMOS-compatible and the integration density is limited by the pitch and size of the solder bumps [27, 38].

Wafer bonded in-plane hybrid lasers

With wafer bonding approach, lasers are fabricated after III-V active material is attached to SOI platform. III-V active epitaxy is grown on its own material substrate, which guaranties high growth quality and excellent optical properties. Then, unpatterned III-V wafer is bonded to patterned SOI wafer and thick III-V substrate is removed, leaving only active epitaxy. In this way epitaxial films with low threading dislocation densities are combined with the lattice-mismatched Si substrate. Lasers can then be fabricated using CMOS-compatible processing and their alignment to Si waveguides is done with high precision using standard lithography steps [38]. Light generated in III-V material is coupled into silicon waveguide by evanescent coupling and confinement factor can be engineered by changing the waveguide width [39]. Using this approach, electrically pumped in-plane lasers on SOI platform have been demonstrated based on various designs such as standard Fabry-Perot cavity [40, 41] and distributed feedback (DFB) [42, 43] lasers, very compact microring [44] and microdisc [45, 46] lasers, as well as very low threshold photonic crystal (PhC)-based lasers [47, 48].

Short-wavelength hybrid vertical-cavity lasers

While previously mentioned types of lasers are in-plane types and therefore potential candidates for on-chip optical interconnect application, vertical-cavity lasers (VCLs) integrated on Si have also been pursued. GaAs-based VCSEL lasing at short wavelength of 845 nm have been demonstrated using wafer bonding [49]. In order for VCLs to be used for on-chip application light needs to be coupled into an in-plane waveguide. This can be achieved efficiently by introducing a diffraction grating to the waveguide layer inside the cavity [50] or on top of the cavity [51]. Similar laser as presented in [49], but incorporating weak diffraction grating inside the cavity, have been numerically investigated [52] and demonstrated [53] recently. These SW-VCLs are not suitable for use with silicon waveguides due to absorption of wavelengths below 1.1 μm in Si, but are potential light source for silicon nitride (SiN) waveguide platform.

Long-wavelength hybrid vertical-cavity lasers

LW-VCLs are attractive for integration with Si-photonics platform for applications in on-chip interconnects and other Si-related technologies due to compatibility of their wavelength with low optical absorption in silicon [13]. However, the DBR issue of InP-based VCSELs mentioned before made implementation of such lasers on the Si difficult as it introduces challenging topography for integration with silicon processing. More fundamental change in LW-VCL design was needed.

This change came in a form of an alternative mirror for vertical resonators: a high-index-contrast subwavelength grating [54, 55]. Offering broadband high reflectivity but in the form of a compact single layer structure, it solves the problems of thick epitaxial DBRs while also offering a range of novel properties. VCSELs employing high-index-contrast grating (HCG) as a top mirror have been numerically investigated [56] and demonstrated for short [57] and long wavelengths [58]. Not long after, the potential of HCG for hybrid VCLs has been recognized and investigated. HCG incorporated into Si can act as a bottom mirror for wafer bonded VCLs forming a hybrid cavity where field extends in both III-V and Si layers. Hybrid HCG-based LW-VCSELs have been demonstrated [59, 60]. Unique property of HCG to couple a portion of the light laterally to the adjacent waveguide has opened the doors for hybrid Si vertical-cavity lasers with in-plane emission [61]. Such lasers have been investigated [60, 62] and demonstrated [63, 64]. With potential to achieve excellent performance in terms of speed and energy efficiency, the hybrid HCG VCLs could be most promising candidates for on-chip optical interconnects.

1.3 Recent progress of VCSELs

Oxide-confined VCSELs emitting around 850 nm are commercially available for almost two decades now [65]. VCSEL-MMF technology continued to dominate short reach optical interconnect markets, with their performance improving to satisfy the bandwidth needs as the serial rate for MMF links increased from 1 Gb/s in 1998 to 10 Gb/s in 2002 and 25 Gb/s in 2015. Currently, GaAs-based 850 nm MM-VCSELs for operation at 25 Gb/s (Ethernet) and 28 Gb/s (Fibre Channel) are in production [66]. Next serial rate, expected to be implemented in 2019, is 50 Gb/s [67]. This has driven a large interest in pushing the performance of the VCSELs further to keep up with and stay ahead of the demand [68].

Apart from increasing data rates, future VCSELs need to be capable to maintain the high modulation speed at high temperatures without adjusting the operating parameters. The lasers are typically placed directly near the data source on-board, inside the module or even directly on chip. The heat dissipation in the systems leads to an operating environment reaching temperatures of 85 °C, even with advanced cooling technologies [69].

In order to reach high data rates, 3-dB frequency bandwidth of the lasers needs to be increased. However, this increase should not be done on the account of increase of driving current. The figure of merit to reflect the simultaneous requirements on the current and speed is modulation current efficiency factor (MCEF), defined as the slope of the change of 3-dB frequency with square root of the bias current [70]:

$$\mathrm{MCEF} \equiv \frac{f_{3\mathrm{dB}}}{\sqrt{I - I_{\mathrm{th}}}}, \tag{1.1}$$

where $f_{3\mathrm{dB}}$ is 3-dB frequency of a small-signal response spectrum, I is driving current and I_{th} is threshold current of the laser. A laser diode structure with a higher MCEF may achieve a target speed at a lower current, which means higher energy efficiency, less self-heating and therefore higher reliability.

As a figure of merit for energy efficiency, we can define heat-to-data ratio (HDR) as [71]:

$$\mathrm{HDR} \equiv (P_{\mathrm{el}} - P_{\mathrm{opt}})/\mathrm{BR}, \tag{1.2}$$

where $P_{\mathrm{el}} = V \cdot I$ is total consumed power at the lasers operating bias point, P_{opt} is optical output power and BR is bitrate. HDR is usually expressed in units of fJ/bit.

Following is non-exhaustive review of progress of VCSEL technology within last decade that inspired or is relevant for the work in this project. Results that are discussed are mostly demonstrated using direct non-return-to-zero (NRZ) modulation. Data rates and distances can be further increased using equalization, forward-error-correction (FEC), digital signal processing (DSP), and multilevel modulation formats such as PAM-4. This not desirable, as it would increase the power consumption, complexity of transmitters/receivers and the cost.

1.3.1 Short-wavelength VCSELs

Most prominent advancement of 850 nm VCSELs in recent years comes from the research group from the Chalmers University of Technology in Sweden. Their lasers employ compressively strained InGaAs/AlGaAs quantum wells (QWs) as active region and the approach to minimize the parasitic oxide capacitance by multiple oxide apertures in the AlGaAs DBR. In 2011 they demonstrated lasers with 3-dB frequency bandwidth of 23 GHz by controlling the photon lifetime by a shallow-surface etch that lowers the reflectivity of the top mirror [72]. With that design they reached 40 Gb/s transmission at room temperature in back-to-back (BTB) configuration [73]. By reducing the cavity to 0.5λ and improving conductivity of DBRs they increased the bandwidth to 27 GHz and demonstrated bit-rates up to 47 Gb/s at room temperature and, more importantly, to 40 Gb/s at 85 °C in 2013 [74]. This result was further pushed to 57 Gb/s at room temperature by optimizing photon lifetime for better large signal transmission [75]. In 2015 they demonstrated further improvement of bandwidth up to 30 GHz and MCEF of 20.6 GHz/mA$^{1/2}$ for lasers with small 3.5 μm aperture, which enabled record HDR below 100 fJ/bit up to 50 Gb/s speeds [76].

Further speed improvements were demonstrated using two tap feed forward equalization (FFE). In collaboration with IBM, using transmitter and receiver equalization, they demonstrated 64 Gb/s over 57m of OM4 MMF in 2014 [77] and 71 Gb/s in 2015 [78].

Other than Chalmers, high-speed 850 nm VCSELs have also been developed by researchers from IBM and Finisar, who demonstrated 56.1 Gb/s optical link in 2013 using VCSEL with 24 GHz 3-dB bandwidth [79].

Researchers from the Technical University of Berlin (TU Berlin) have demonstrated some very energy-efficient 850 nm VCSELs. In 2012 they published results showing HDR of 56 fJ/bit for error-free performance at 25 Gb/s using single mode VCSELs with 3.5 μm aperture in a BTB test configuration [80]. Next year they demonstrated 40 Gb/s with low dissipated HDR of only 108 fJ/bit [81].

Major progress with high-speed 980 nm VCSELs came from the University of California in Santa Barbara (UCSB) who demonstrated bottom-emitting, tapered oxide apertured VCSELs with strained InGaAs/GaAs QWs. They reached 35 Gb/s operation from lasers with 20 GHz bandwidth and MCEF of 16.7 GHz/mA$^{1/2}$ in 2009 [82]. Group from TU Berlin first presented 44 Gb/s operation at room temperature and 38 Gb/s at 85 °C from top side emitting 980nm VCSEL with InGaAs/GaAsP QWs and 1.5λ cavity in 2011 [83]. By reducing the cavity to 0.5λ and tuning the photon lifetime, in 2014 they reported the laser with 24.7 GHz modulation bandwidth and great temperature stability. They achieved 46 Gb/s at 85 °C [84]. Most recently they used deposition of thin films of Si_xN_y on top of the complete processed VCSEL wafer pieces to precisely tune the photon lifetime and in 2016 they presented lasers with 26.6 GHz bandwidth and great temperature stability which operated at 50 Gb/s at temperatures from 25 °C to 85 °C [85]. Even though these results are close to best 850 nm VCSELs, their energy efficiency is still slightly worse with best HDR of 280 fJ/bit. Most recently, they demonstrated 31 GHz bandwidth from single mode lasers with very small apertures of 1.5 μm [86].

1060 nm VCSELs have only more recently came into focus as a potential solution for extending the reach beyond several hundreds of meters that is limit for 850 and 980 nm lasers. Without going to longer wavelengths and InP-based lasers, the GaAs-based VCSEL technology can be extended to about 1100 nm where the chromatic dispersion is one third of that at 850 nm and attenuation is below 1 dB/km. This could potentially serve as solution for medium distance optical links. Notable recent work on 1060 nm VCSELs was done by Furukawa. In 2014 they demonstrated low-resistance high-efficiency oxide-confined VCSELs with InGaAs/GaAs QWs, double intra-cavity structure and dielectric top DBR that had 20 GHz modulation bandwidth and enabled 28 Gb/s transmission up to 75 °C [87]. Next year, they reached 1 km transmission at 25.78 Gb/s using 1060-nm specialized MMFs. Most recently the group from Chalmers has adapted their 850 nm VCSEL design for 1060 nm. They used strain-compensated InGaAs/GaAsP QWs in their VCSEL design with short optical cavity and multiple oxide apertures. In 2018 they reported 22 GHz bandwidth from single mode design and demonstrated 50 Gb/s at 25 °C and 40 Gb/s at 85 °C in BTB configuration with dissipation of 100 fJ/bit. With prototype 1060 nm optimized MMF and mode-selective launch they demonstrated 25 Gb/s transmission over 1 km [88].

1.3.2 Long-wavelength VCSELs

In order to overcome low index contrast of InP-based epitaxial DBRs, two hybrid mirror technologies have been developed [65]. One is to use dielectric DBRs which can be made from materials with much higher refractive-index contrast. This reduced thickness of DBRs and improved speed, however dielectric materials often mean low thermal conductivity which limits the high temperature operation. The second approach is wafer fusing of Al(Ga)As/GaAs DBR mirrors [13]. With such mirrors, good electrical and thermal conductivity can be achieved. The problem is high cost of fabrication due to high wafer consumption.

LW-VCSELs often employ tunnel junction (TJ) to avoid a highly-resistive p-type InP or InGaAs contact layers [89, 90]. With TJ, hole current can be converted to electron current so the contact layer on p-side of the laser diode can also be n-type, with lower electrical and optical losses. Best performance was achieved by lasers that implement buried tunnel junction (BTJ), which is

achieved by patterning TJ layers before rest of the epitaxy is grown. In this way excellent electrical confinement is ensured [91].

Most successful high-speed LW-VCSELs originate from research groups from Technical University of Munich (TUM) and Vertilas. Their design featured BTJ and cavity formed between epitaxial InGaAlAs DBR and dielectric DBR mirror. The structure is then electroplated with Au to form a heatsink on the dielectric mirror side (forming a hybrid mirror), flipped and the substrate is removed so that light emission is from the epitaxial mirror side. Thanks to the integrated heatsink, the lasers had excellent temperature performance. With this design they demonstrated 10 Gb/s data transmission over 4.6 km at 1.55 μm wavelength from lasers with 8 GHz bandwidth in 2006 [92]. Together with researchers from TU Berlin and University of California at Berkeley, they showed open eyes at 22 Gb/s and the first error-free data-transmission at 12.5 Gb/s up to 85 °C in 2009 [93] using lasers with 12 GHz bandwidth that uses design planarized with BCB to form coplanar contact pads. Not long after, they replaced top epitaxial mirror with another dielectric mirror. Higher refractive-index contrast results in shorter penetration depths and therefore shorter effective cavity length [94]. Top contact is then also formed intra-cavity which improved heat flow from active region further reducing the thermal resistance of the device. Short-cavity laser presented in that work showed modulation bandwidth of 15 GHz and MCEF of 8.2 GHz/mA$^{1/2}$ at 25 °C and good temperature stability. With this design, in 2010, error-free transmission at 35 Gb/s in BTB configuration and 25 Gb/s over 4.2 km of standard SMF at room temperature was demonstrated [95]. In the same year, from another laser they got maximum 3-dB bandwidth of 19 GHz and MCEF of 11.3 GHz/mA$^{1/2}$ and were able to perform data transmission at 40 Gb/s in BTB configuration for the first time [96]. Vertilas also partnered with IBM and, using the same driver IC with two-tap FFE used in [78] to achieve error-free 71 Gb/s transmission with the 850 nm VCSEL, demonstrated a directly NRZ modulated 1530 nm VCSEL link operating error-free to 56 Gb/s BTB and 50 Gb/s to 2 km of large effective area fiber (LEAF) [97]. This is the highest data rate demonstrated for a C-band VCSEL to date. Most recently, in 2016, group from TUM reported VCSELs with 1.5λ short cavity, single mode emission and bandwidth in excess of 21 GHz [98]. Data rates of 50 Gb/s were demonstrated in BTB configuration without FFE or equalization.

LW-VCSEL design from TUM and Vertilas has been adapted not only for 1.55 μm window, but for a wide wavelength range from 1.3 μm up to 2.3 μm [99]. The active region of their 1.3 μm VCSELs consists of five compressively strained quantum wells based on the InGaAlAs material system. The Al-content of the wells is 18%, which is more than twice as high than that of comparable 1550 nm. Major progress of 1.3 μm VCSELs came in 2012 by adapting short-cavity concept from [94]. They were able to demonstrate lasers with 15 GHz 3-dB frequency and MCEF of 11.9 GHz/mA$^{1/2}$ [100]. Not long after, together with researchers from TU Berlin, with this laser they demonstrated 25 Gb/s error-free data-transmission at room temperature over 25 km [101] and 30 Gb/s over 10 km [102].

LW-VCSELs have also been researched by the group from Ecole Polytechnique Fédérale de Lausanne (EPFL), who employed double wafer-fused heterostructures [103]. In their design, InP based active layer is sandwiched between two undoped GaAs/AlGaAs DBRs, with intra-cavity contacts and top side emission. They improve modulation bandwidth by increasing the differential gain provided by the active region using larger strain in the QWs and tuning the cavity photon lifetime. Recently, in 2016, they presented the 1310 nm VCSELs with modulation bandwidth of up to 11.5 GHz by increasing the strain in the InAlGaAs/InP QWs to 1.6% and adjusting the number of pairs in the DBRs [104]. They achieved 25 Gb/s error-free operation over 10 km. These results show high-speed and high efficiency potential for wafer-fused LW-VCSELs.

Without aid from FEC, DSP and advanced modulation formats, if we aim to reach 100 Gb/s, both the VCSEL and photodiode would need significant increase in bandwidth (up to the 40 GHz level) [78]. It is a question if the current state-of-the art technology can achieve this.

1.3.3 HCG and hybrid VCSELs

A high-index-contrast grating (HCG) is a grating in which there is a large refractive-index contrast between the grating bars and materials that surrounds them. It can act as a broadband high

reflectivity mirror [54, 55], and has quickly found application as a mirror for VCSELs [56]. They can be very compact single layer structure, which makes it attractive alternative for thick epitaxial DBRs or even dielectric DBRs. Due to their strong field confinement ability, they have very short energy penetration depth [105], which gives smaller mode volume of the laser. Also, phase penetration depth, which relates to photon lifetime, can be tuned without degrading the reflectivity [106], unlike with shallow etching method as used in [72] for example. Smaller mode volume and control of photon lifetime are essential for achieving high modulation speed, thus HCG has potential to improve performance of VCSELs [106].

First demonstrations of VCSELs employing HCG as a mirror came in 2007 from two groups independently: group from University of California at Berkeley (UC Berkeley) who demonstrated short-wavelength GaAs-based electrically pumped laser [57], and group from Lyon Institute of Nanotechnology (INL) who demonstrated long-wavelength InP-based optically pumped laser [58]. Both designs feature conventional bottom epitaxial DBR mirrors and a top HCG realized as III-V membrane surrounded by air by doing sacrificial etching of layer beneath the grating layer.

Group from UC Berkeley remained the leader in developing HCG VCSELs in following years. Early on their investigations showed excellent transverse single mode properties [107], strong polarization selectivity and good fabrication tolerance [108] thanks to HCG. They also first exploited HCG suspended in air for wavelength tuning by integrating the HCG with nanoscale actuators to create a mobile and lightweight reflector. Such nanoelectromechanical optoelectronic (NEMO) tunable VCSELs showed 3-dB frequency bandwidth for tuning of 3.3 MHz (∼40–50 times faster wavelength tuning speed compared with existing DBR-based tunable VCSELs) [109]. By exploiting thinner HCG design for transverse electric (TE) polarization, they improved the speed up to 7.9 MHz [110]. In 2010 they collaborated with group from TUM to integrate HCG into their short-cavity BTJ LW-VCSELs shown in [94]. They replaced top dielectric DBR with SiO_2 spacer and amorphous Si, in which HCG was defined, and demonstrated first electrically pumped VCSEL in 1.3 μm wavelength range with high polarization mode selectivity and improved higher order transverse modes suppression [111]. While largest apertures for DBR VCSELs that were single mode was 8 μm, with HCG lasers were single mode for up to 12 μm apertures. However, due to growth related issues these devices showed much higher threshold and poorer thermal performance compared to reference design shown in [94]. In the same year, from their own design they reported first 1.55 μm InP-based HCG VCSEL operating CW at temperatures up to 60 °C [112]. In this device design, BTJ is not implemented in order to keep epitaxy to single step and lower the cost. Instead, current confinement is achieved using proton implantation. The lasers showed excellent single mode emission and low thermal resistance. Couple of years later, they showed tunable version with electrostatically-actuated NEMO HCG [113]. Tuning range of 26.5 nm was achieved using combined mechanical and thermal tuning. The lasers presented then also showed good modulation performance, with the 3-dB bandwidth of 7.5 GHz, and they demonstrated error free direct modulation operation up to 10 Gb/s at 20 °C over 100 km fiber link. In 2015, they combined their LW HCG VCSEL design with SOI substrate [60]. In this work, they employ flip-chip eutectic bonding to integrate III-V epitaxy, containing AlGaInAs compressively-strained QWs and epitaxial DBR, onto SOI on which the HCG is fabricated. Eutectic AuSn thin film is patterned on SOI so that air gap is left above the grating that would be hermetically sealed after the bonding. The air gap length is controlled by controlling the thickness of the metal film during fabrication. The lasers operated CW up to 60 °C with single transverse and longitudinal mode emission. The modulation bandwidth was measured to be 2.5 GHz, limited by parasitics, and they were able to achieve error free operation up to 5 Gb/s at 20 °C. In [60] they also numerically investigated in-plane coupling to Si waveguide using HCG. Most recently, the UC Berkeley group showed tunable VCSEL with HCG in 1060 nm wavelength range [114] and explored two-dimensional HCGs [115].

Research group from INL focused on heterogeneously integrated 1.55 μm vertical cavity lasers that employ Si HCG (which they refer to as photonic crystal mirror (PCM)). In 2011 they presented first realization of a long-wavelength VCSEL where both mirrors are HCGs [59]. Heterogeneous integration is done using direct molecular bonding, so InP/InGaAsP heterostructure is embedded between two Si/SiO_2 grating mirrors. The gratings contained heterostructures for optical confinement. The lasers showed single mode CW operation at room temperature despite low

thermal conductivity of SiO_2 that surrounds active region. Heat sinking paths are through the III-V active layers since no lateral structuring is done. They were able to adapt this design for electrical pumping also and demonstrate in-plane coupling to Si waveguide [63]. The electrically pumped version uses tunnel junction and proton implantation for current confinement.

The third notable group that investigated HCG VCSELs is group from DTU Fotonik, part of which is the author of this thesis and where this work has been done. In early work, published in 2008, in collaboration with researchers from CEA-Leti, they showed that transverse magnetic (TM) HCG is advantageous for laser design as it requires thinner low refractive-index layer [116]. Investigation was done on short-wavelength VCSELs with TM HCG that uses oxide gap instead of air-gap-based structures demonstrated previously [117]. With the oxide-based structure fabrication would be simpler and the grating would have better mechanical stability. Lasers based on that design have been demonstrated in 2010 [118], and CW lasing was shown at temperatures up to 70 °C. The DTU Fotonik group then focused on hybrid III-V-on-Si VCL that employ HCG both as a bottom mirror and as an in-plane coupler [62]. The investigated structure has Si HCG and adjacent waveguide fabricated on SOI wafer, wafer bonded III-V active epitaxy with InAlGaAs QWs for 1.3 μm emission, dielectric top DBR and intra-cavity contacts. Lasers based on this design were experimentally demonstrated with optical pumping in 2015 [64]. III-V active layer used for this demonstration was 1λ thick and included 7 InGaAlAs/InGaAlAs strained QWs emitting near 1.5 μm. Efficient in-plane emission was characterized. High-speed potential of the design was recognized and investigated. By employing TM HCG, thickness of low index material, in this design air gap, can be significantly smaller compared to TE HCG, due to shorter evanescent tail [119]. Together with high-index-contrast dielectric DBR, very high confinement factor of 12.2% is achieved and modulation speed of the laser can be enhanced. High-speed optically pumped VCSEL based on this design was demonstrated, lasing single mode at 1.54 μm. It showed 3-dB frequency bandwidth of 27 GHz which is the highest reported among Si on-chip lasers. Furthermore, estimated MCEF is 42.1 GHz/mA$^{1/2}$, several times larger than conventional high-speed lasers, showing potential for very efficient high-speed operation [120]. Characterization setup limited the maximum pumping power that could be tested. So, based on obtained experimental results, numerical investigation was done, and potential for much higher intrinsic bandwidth at higher pumping, potentially enabling data rates as high as 120 Gb/s [121].

1.4 Thesis contribution and outline

1.4.1 Subject and contribution of the thesis

The subject of this thesis are long wavelength vertical cavity lasers. From the discussion in this chapter we can recognize their potential for application across large range of optical interconnect types, from several micrometers to several kilometers. They can be promising candidate for on-chip interconnects, with wavelength compatible with Si photonics, or bring advantages of VCSELs to long distance fiber links in mega data centers.

The requirement for such lasers are quite challenging if we are to utilize the current microelectronics and optical communication technologies [27]:

- they must emit in 1310 or 1550 nm wavelength range to be compatible with the existing fiber optical network;
- electrically pumped lasing is necessary for a compact size and high integration density;
- modulation bandwidth must be sufficient for next generation of data rates
- they must display high power efficiency for sufficient output power and low energy cost-per-bit in data transmission;
- integration on Si is desired, with CMOS-compatible fabrication for low-cost and large-scale manufacturing.

No LW-VCSEL demonstrated so far, to the best of authors knowledge, satisfies these requirements sufficiently.

The aim of this work is to experimentally demonstrate a laser that could satisfy outlined requirements. The laser design that is investigated is based on the high-speed lasers demonstrated in [120], which have shown exceptionally good performance and great potential under optical pumping operation. In this work, the design is adapted for electrical pumping and experimental demonstration is pursued, with aim to preserve excellent performance.

The laser structure is hybrid, with InP-based active epitaxy integrated on SOI platform using wafer bonding. The vertical cavity is comprised of bottom HCG, formed in Si layer of SOI, and dielectric DBR deposited and patterned at the end of device fabrication. Compared to optically pumped version, design is adapted for electrical pumping. Doped layers and TJ are incorporated into the epitaxy and contacts are formed in intra-cavity scheme. Proton implantation and undercut etching are investigated as methods for carrier confinement. In this work, focus is on vertical surface emission, so no Si waveguide structures are included and no in-plane characterization is done. However, as demonstrated in [64], the design can be adapted for in-plane emission also.

Some of the challenges that were tackled over the course of this project were:

- development of adhesive wafer bonding method as an alternative to previously used direct wafer bonding;
- investigation of carrier confinement methods: proton implantation and undercut etching;
- investigation of ohmic contacts, with focus of lowering the resistance and eliminating deep metal diffusion;
- reduction of electrical parasitic elements;
- electrical pumping characterization of fabricated devices.

While these challenges are known in literature and have been investigated by various groups before, adapting and reproducing the state-of-the-art solutions was challenging and time consuming. It was often necessary to start with most basic tests and learn along the way. The hybrid approach made some of the most common solutions difficult to implement, therefore alternative methods needed to be explored.

The fabrication processes used in this work to fabricate the lasers are CMOS-compatible. Almost all of the fabrication is done in state-of-the-art cleanroom at DTU Danchip, with the exception of proton implantation that was outsourced. Development and optimization of processes for wafer bonding, implantation, ohmic contact formation, lithography, planarization and others, has been done. Process for adhesive wafer bonding using ultra-thin polymer layer has been reproduced from literature with high yield. In early testing, issue with deep diffusion of gold during ohmic contacts fabrication was discovered and, as a solution, a two-step metallization approach was adapted and specific contact resistance was demonstrated to be as good as state-of-the-art values.

The III-V epitaxies used for fabricating VCSELs in this work were obtained from outside suppliers, with active region and tunnel junction designs developed by them. Due to long waiting times, high price, limited supply and availability, it was sometimes necessary to work with epitaxies that have one or more issues. Insufficient gain, high TJ series resistances, deviation from design, poor surface quality and particles are some of the problems that had to be handled.

Several versions of full VCSEL design have been fabricated and characterized. First version showed excellent TJ properties, but no light emission has been observed. This was shown to be due to issue with active region, which was unable to emit any light under electrical pumping. Two versions were fabricated using different epitaxy which showed good light emission when tested but had higher differential resistance. However, no lasing was observed from VCSELs due to issues with epitaxial design deviation and poor fabrication yield caused by poor surface quality. Fourth version was based on epitaxy without TJ, but with improved surface quality. The fabrication results were improved; however, no lasing was observed. While spontaneous emission that was observed showed distinctive peak in the spectrum, it was below the lasing threshold. The lack of lasing result is attributed to a number of factors, and further optimization of the design is necessary.

1.4.2 Structure of the thesis

The content of this thesis is organized in seven chapters, as follows:

Chapter 1, Introduction, describes general motivation for this work and introduces optical interconnects, their potential and requirements. Role of silicon photonics is discussed and different technologies for lasers on silicon are reviewed. Advantages of VCLs are highlighted and review of the recent progress of different VCSELs technologies is given.

Chapter 2, Theory and optical design, gives theoretical overview of optical design of the laser. Theory behind HCGs is shortly discussed and different mirror technologies for VCSELs are compared. High-speed design is discussed and described in more details.

Chapter 3, Electrical pumping of VCSELs, introduces considerations for electrical pumping for high-speed. Requirements for achieving good performance are discussed and methods for current confinement, including implantation and lateral etching, are studied. Furthermore, optimization of ohmic contacts is summarized and experimental results are given.

Chapter 4, Device designs, describes the details of the laser design. Detailed description of the VCSEL structure is given and different laser versions, designs and epitaxies are discussed.

Chapret 5, Wafer Bonding of III-V to SOI, introduces the wafer bonding technologies that were investigated and used for heterogenous integration of III-V on Si platform. Direct and adhesive wafer bonding methods are discussed in detail. The experimental testing of ultra-thin BCB adhesive bonding is described and stable bonding recipe is given.

Chapter 6, Fabrication of hybrid VCSELs, covers the fabrication process. Short overview of the process flow is provided and then important specific processes are described in more detail. Experimental issues and solutions will be presentet.

Chapter 7, Results and discussion, describes the characterization setups, summarizes the fabrication results and reports the results of the laser characterization for several versions of the proposed laser.

Chapter 8, Conclusion and Outlook, summarizes the main results of this thesis and gives an outlook on further work.

CHAPTER 2

Theory and optical design

2.1 Introduction

Semiconductor laser physics is very complex, requiring understanding of optical, electrical and thermal phenomena for full description of laser operation [122–125]. All of these phenomena are coupled and interact between each other, and to get a complete picture of a laser all of them should be modeled together, including quantum mechanical description of the active region. Such advanced models are exceptionally demanding and outside of the scope of this thesis. In most cases, simpler models that consider optical, electrical and thermal properties separately can be enough to design and analyze the VCSELs.

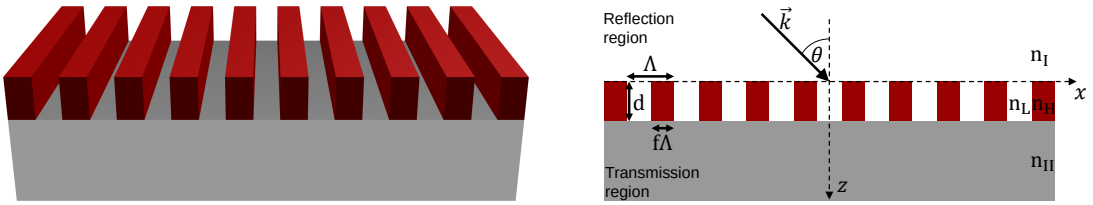
Achieving excellent performance from a laser requires optimization of optical design of the laser, efficient electrical injection and excellent thermal properties. Designs based on previously demonstrated and proven approaches can be optimized, efficiency improved and limits of the performance pushed, but more significant improvements often come from using innovative approaches. Oxidation of Al-rich layers, short-cavity designs, dielectric mirrors, heat-sinks, tunnel junctions, etc., are all examples of innovative technologies that boosted the VCSEL performance in different regards.

In this chapter, the optical design of the proposed laser is considered. The key innovation in this design is the HCG, optimized for achieving fast intrinsic frequency response of the laser. Some main theoretical concepts of HCG will be described, focusing on application as a reflector. Different mirrors designs for VCSELs are reviewed and theoretically compared. Basic theory of dynamic properties of lasers and high-speed design will be given and discussed, including the design of VCSEL used in this work.

2.2 High-index-contrast grating

Optical gratings are structures with periodic change of the refractive index. They can have one-, two- or three-dimensional spatial periodicity and, depending on the ratio of grating period and incident light wavelength, can exhibit different optical properties.

A high-index-contrast subwavelength grating (HCG) is a class of one-dimensional (1D) gratings in which grating period is close to the wavelength of incident light and there is a large refractive-index contrast between the grating bars and materials that surrounds them in all directions [126]. Such gratings show unique and extraordinary properties that are not possible with conventional diffraction gratings. They are polarization selective and can be designed to have high reflectivity ($> 99\%$) over a broad bandwidth [54, 55] or high quality (Q) factor resonances ($Q > 10^7$) [127, 128]. They have found application in numerous devices. Main application is as a novel mirror for VCSELs, both fixed and MEMS, but also for beam steering or focusing [129, 130]. Ultra-high Q-factor resonances are employed to make HCG-resonator lasers with surface normal emission. In this work, HCG is used in its most common role, as a reflector in vertical cavity laser structure.



(a) **(b)**

Figure 2.1: (a) Schematic illustration of the 1D grating structure. (b) Schematic cross-sectional view showing parameter definitions and incident beam.

In order to explain the physics of the HCGs, it is necessary to start from the basics of the gratings and diffraction. With better understanding of the mechanisms that lead to the unique properties of the HCGs, it will be easier to optimize their design.

2.2.1 Subwavelength gratings

A schematic illustration of HCG is shown in Fig. 2.1. The incident/reflection region, with refractive index n_I and transmission region, with refractive index n_{II}, are separated by a grating structure. The grating is comprised of bars of high refractive-index material (n_H) with low refractive-index material (n_L) between them. The period of the grating is Λ and the bar width is fΛ, where f is called filling factor or duty cycle. The thickness of the grating is d. For basic analysis, it is assumed that grating extends infinitely in y-direction and is infinitely periodic in x-direction.

Diffraction on the grating

To understand fundamental properties and different regimes of diffraction on optical gratings, a simple grating equation can be considered.

An incident plane wave hitting the grating at the incident angle θ from z-axis, as illustrated on Fig. 2.1b, can be expressed as:

$$E_{\mathrm{inc},y} = \exp(-\mathrm{j}\vec{k}\cdot\vec{r}) \tag{2.1}$$

assuming normalized TE polarized light and time dependency of $\exp(-\mathrm{j}\omega t)$. Here $\vec{k} = \mathrm{k_0 n_I}(\hat{x}\sin\theta + \hat{z}\cos\theta)$ is the wave vector in incident medium n_I, with wavelength in vacuum λ_0 and wave number $\mathrm{k_0} = 2\pi/\lambda_0$.

Depending on the angle, wavelength of the incident light and refractive indices, multiple reflected and transmitted orders could be excited as defined by a grating equation:

$$k_{x,m} = k_{x,\mathrm{inc}} - m\mathrm{K}, \quad m = 0, \pm1, \pm2, \cdots, \tag{2.2}$$

where m is diffracted order number, $k_{x,m}$ is x-component of the diffracted beam wave vector, $k_{x,\mathrm{inc}} = \mathrm{k_0 n_I}\sin\theta$ is x-component of the incident beam wave vector, and $\mathrm{K} = 2\pi/\Lambda$ is grating wave number. It should be noted that $k_{x,m} = \mathrm{k_0 n_I}\sin\theta_{m,I}$ in reflected region and $k_{x,m} = \mathrm{k_0 n_{II}}\sin\theta_{m,II}$ in transmitted region, meaning that the angles of the beams are different in two different regions. The Eq. (2.2) can be rewritten for reflected and transmitted beams, respectively, in following way:

$$\mathrm{n_I}\sin\theta_{m,\mathrm{I}} = \mathrm{n_I}\sin\theta - m\frac{\lambda_0}{\Lambda}, \quad m = 0, \pm1, \pm2, \cdots, \tag{2.3a}$$

$$\mathrm{n_{II}}\sin\theta_{m,\mathrm{II}} = \mathrm{n_I}\sin\theta - m\frac{\lambda_0}{\Lambda}, \quad m = 0, \pm1, \pm2, \cdots, \tag{2.3b}$$

and also illustrated using phase-matching diagram as shown in Fig. 2.2. From Eqs. (2.3) we can see that the m^{th} diffracted mode will be propagating only if the $\sin\theta_m$ is smaller than one. All higher modes that do not satisfy this condition will not be able to propagate in z-direction

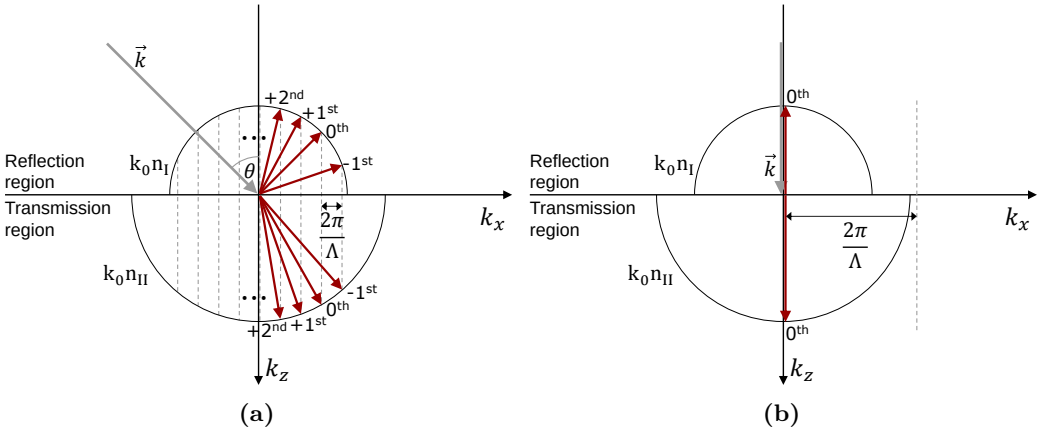


Figure 2.2: (a) Phase-matching diagram of a grating supporting several diffraction order beams. (b) Phase-matching diagram for a subwavelength HCG with normal incident beam, showing that condition is satisfied for only 0^{th} order.

outside of the grating, they will be evanescent. Gratings with period $\Lambda > \lambda_0/\mathrm{n_{I,II}}$ are conventional diffraction gratings with several diffracted beams in reflected or transmission region. On the other side, gratings with period $\Lambda < \lambda_0/\mathrm{n_{I,II}}$ are called subwavelength gratings. For such gratings, with normal incident beam ($\theta = 0$) all diffracted orders with $m \neq 0$ are evanescent in both regions, and only 0^{th} order can propagate, as illustrated on Fig. 2.2b. Finally, gratings with $\Lambda << \lambda_0/\mathrm{n_{I,II}}$ are called deep-subwavelength gratings and they appear as a homogeneous medium with an effective refractive index [131].

Rigorous coupled-wave analysis

One of the methods that is commonly used for numerical investigation of diffraction of electromagnetic waves by periodic structures is rigorous coupled-wave analysis (RCWA). In this method, Maxwell's equations are solved in spatial frequency domain. Fourier series expansion with spatial harmonics of the fundamental spatial frequency is used for permittivity of the grating structure and the fields that interact with it [132]. The accuracy of the solution obtained depends only on the number of terms in the expansion.

The periodic relative permittivity in the grating region can be expanded as

$$\varepsilon(x) = \varepsilon(x + n\Lambda) = \sum_m \varepsilon_m \exp\left(\mathrm{j}\frac{2\pi}{\Lambda}m\right), \quad -\infty \leq m \leq \infty, \tag{2.4}$$

where ε_m is m^{th} Fourier harmonic. In practical numerical simulations, number of harmonics is limited to $-M \leq m \leq M$. For a simple square grating, the Fourier harmonics are given by:

$$\varepsilon_0 = \mathrm{n_H}^2\mathrm{f} + \mathrm{n_L}^2(1-\mathrm{f}), \quad \varepsilon_m = (\mathrm{n_H}^2 - \mathrm{n_L}^2)\frac{\sin(m\pi\mathrm{f})}{m\pi}. \tag{2.5}$$

In the following TE polarized incident field is assumed as given by Eq. (2.1). TM polarized light, can be expressed similarly using $H_{\mathrm{inc,y}}$ field. The incident field can be rewritten as:

$$E_{\mathrm{inc},y} = \exp\left[-\mathrm{j}k_0\mathrm{n_I}(x\sin\theta + z\cos\theta)\right]. \tag{2.6}$$

The fields in reflection region ($z < 0$) and transmission region ($z > d$) can be expressed in expanded form as:

$$E_{\mathrm{I},y} = E_{\mathrm{inc},y} + \sum_m R_m \exp\left[-\mathrm{j}(xk_{x,m} - zk^{\mathrm{I}}_{z,m})\right], \quad z < 0, \tag{2.7a}$$

$$E_{\mathrm{II},y} = \sum_m T_m \exp\left[-\mathrm{j}(xk_{x,m} - (z-d)k^{\mathrm{II}}_{z,m})\right], \quad z > d, \tag{2.7b}$$

where R_m and T_m are normalized amplitudes of m^{th} reflected and transmitted diffracted field, respectively, $k_{x,m}$ is determined by Eq. (2.2), and z-component of wave vector is given by dispersion relation:

$$k_{z,m}^{\text{i}} = \begin{cases} +\sqrt{(\text{k}_0\text{n}_\text{i})^2 - k_{x,m}^2} & \text{if } \text{k}_0\text{n}_\text{i} > k_{x,m} \\ -\text{j}\sqrt{k_{x,m}^2 - (\text{k}_0\text{n}_\text{i})^2} & \text{if } \text{k}_0\text{n}_\text{i} < k_{x,m} \end{cases}, \quad \text{i} = \text{I}, \text{II} \tag{2.8}$$

The magnetic fields can be obtained from Maxwell's equation

$$H = \left(\frac{\text{j}}{\omega\mu_0}\right) \nabla \times E. \tag{2.9}$$

The fields in the grating region ($0 < z < d$), may be expressed in similar way:

$$E_{\text{g},y} = \sum_m S_m(z) \exp\left[-\text{j}(xk_{x,m})\right], \tag{2.10a}$$

$$H_{\text{g},x} = -\text{j}\left(\frac{\varepsilon_0}{\mu_0}\right)^{1/2} \sum_m U_m(z) \exp\left[-\text{j}(xk_{x,m})\right], \tag{2.10b}$$

where $S_m(z)$ and $U_m(z)$ is normalized amplitude of m^{th} space-harmonic field in the grating region and $k_{x,m}$ is defined by Eq. (2.2). These fields must satisfy Maxwell's equations:

$$\frac{\partial E_{\text{g},y}}{\partial z} = \text{j}\omega\mu_0 H_{\text{g},x}, \tag{2.11a}$$

$$\frac{\partial E_{\text{g},y}}{\partial x} = -\text{j}\omega\mu_0 H_{\text{g},z}, \tag{2.11b}$$

$$\frac{\partial H_{\text{g},x}}{\partial z} = \text{j}\omega\varepsilon_0\varepsilon(x) E_{\text{g},y} + \frac{\partial H_{\text{g},z}}{\partial x}. \tag{2.11c}$$

After substituting Eqs. (2.10) into Eqs. (2.11) and solving, we can obtain coupled wave equations:

$$\frac{\partial S_m}{\partial z} = \text{k}_0 U_m, \tag{2.12a}$$

$$\frac{\partial U_m}{\partial z} = \frac{k_{x,m}^2}{\text{k}_0} S_m - \text{k}_0 \sum_p \varepsilon_{m-p} S_p. \tag{2.12b}$$

This system of differential equations can be solved using matrix formalism to obtain eigenvalues and eigenvectors that describe the fields inside the grating. The diffracted fields outside grating, R_m and T_m, can be obtained by matching the tangential electric- and magnetic-field components at the two boundaries $z = 0$ and $z = d$.

The derivation presented here is the basis of the RCWA method. Detailed and practical implementation is outside the scope of this thesis. The numerical simulations of the gratings in this thesis have been done using freely distributed RCWA implementation called Rigorous Optical DIfraction Software (RODIS) developed by Photonics Research Group at the University of Ghent, Belgium [133].

Physics of a grating

Physics of the gratings can be interpreted using two different pictures: guided-mode resonance (leaky modes) or waveguide-array mode (Bloch modes).

Guided-mode resonance (GMR) is a well-known phenomenon developed for gratings with low refractive-index contrast [134, 135]. In this picture, grating can be seen as a waveguide with periodic refractive-index modulation which can support guided modes propagating in the lateral x-direction. Diffracted beams, generated when the incident beam hits the grating (see Fig. 2.2a), can couple into the guided modes if the phase-matching condition is satisfied at specific wavelengths.

Light also couples back into the diffracted beams, making them leaky. Therefore, light interaction with a grating can be investigated through the coupling between diffracted modes and GMRs

Second way to describe the gratings is to consider them as a periodic array of short waveguides in the normal z-direction. Waveguide-array modes can be supported and excited by the incident wave [131, 136, 137]. These modes propagate across the grating thickness with different propagation constants and accumulate phase. The grating properties can be investigated by studying these modes and how they couple with themselves, between each other and light outside the grating at the interfaces. Depending on the grating parameters and the wavelength of the incident light, number of supported modes can vary. For deep-subwavelength gratings only one mode is propagating, so the grating is seen as uniform layer with effective refractive index. At longer wavelengths, many modes can interact enabling complex diffraction.

2.2.2 HCG as a broadband reflector

HCGs gained a lot of attention when they were reported to show broadband high reflectivity for surface-normal incident light in 2004 by group of Chang-Hasnain et al. at the University of California, Berkeley [54], who also made the first experimental demonstration in same year [55]. They also developed waveguide-array modes picture as a theoretical explanation of the high reflectivity property of HCG [131, 136, 137].

Origin of reflectivity

Under the conditions that define a HCG, only two waveguide-array modes within the grating can be supported, while outside the gratings only 0^{th} diffraction order mode is propagating in both reflection and transmission region. When the plane wave arrives at the top interface plane of the grating, two modes are excited and they propagate until they reach bottom interface plane. At this second interface the modes are reflected back and coupled between each other. They could also couple to the 0^{th} order diffracted mode in transmission region, but if the interference of the two modes is destructive at this interface, no light is transmitted and high reflection is obtained. If two such high reflection points occur at close wavelengths in the spectrum, the high reflectivity spectrum will be broadband.

The GMR concept can also be used to describe broadband high reflectivity of the HCG [138]. GMRs can cause the dips in the transmission spectrum, and when multiple dips occur close in the spectrum, the reflectivity is high in broad wavelength range.

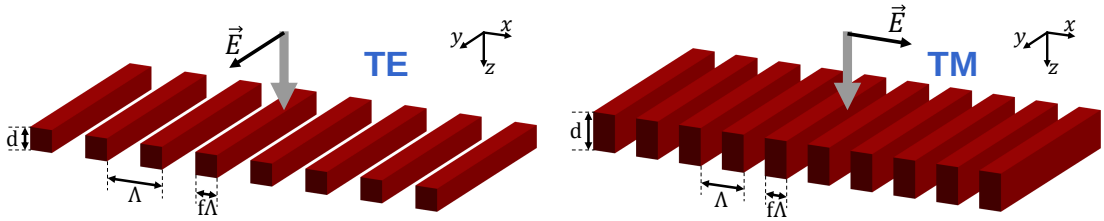
Polarization selectivity

HCGs are by nature sensitive to polarization, due to their 1D periodic structure [57, 119]. Fig. 2.3 shows illustration of HCGs optimized for TE and TM polarized light, and the orientation of the electric field polarization for both cases. Grating optimized for high reflectivity of one polarization will not be highly reflective for the other one. This property is very useful for their application in lasers, as only one polarization will meet lasing condition and the other one will be suppressed, preventing polarization-mode hopping.

Reflectivity spectrums

Properties of HCGs are scalable with wavelength. By simply multiplying the grating dimensions by a constant, same HCG design can be easily scaled to the other wavelength ranges, as long as the refractive index does not change much [54]. Therefore, it is common to use normalized dimensions with respect to the period (i.e. λ/Λ for wavelength) when plotting the reflectivity spectrum of the gratings.

Different grating regimes can be distinctively recognized if we plot reflectivity spectrum of the HCG for varying grating thickness as shown in Fig. 2.4. These contour maps were calculated using RODIS for TE- and TM-polarized incident planar wave, and the structure simulated is silicon ($n_H = 3.48$) grating sitting on the silicon dioxide ($n_{II} = 1.48$) with air above and between

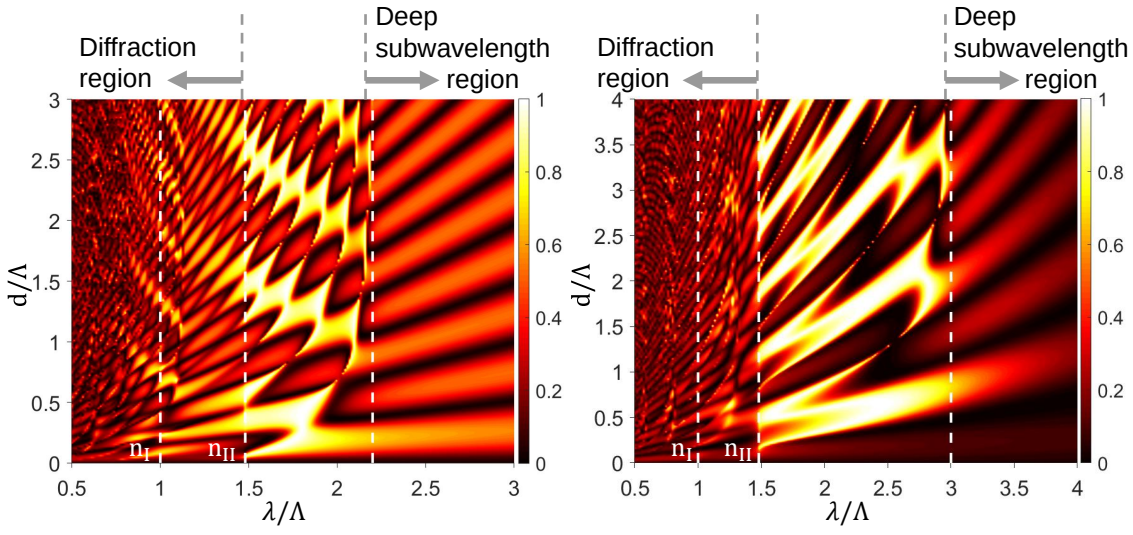


(a) (b)

Figure 2.3: Schematic of the HCG optimized for (a) TE and (b) TM polarized light. Grey arrow represents light propagation direction and black arrow represents the direction of the electric field polarization. For TE polarization, electric field is parallel to the grating bars, while for TM it is perpendicular.

grating bars ($n_I, n_L = 1$). In the contour maps we can recognize the three previously discussed grating regimes. For the long wavelengths, when the grating period is much smaller, we have deep-subwavelength region and the reflectivity is similar to the reflectivity of uniform slab with simple pattern of constructive and destructive interference between the waves reflected between top and bottom interface of the grating. For the short wavelengths, when $\Lambda > \lambda/n_{II}$, the higher order diffracted modes start to appear in transmission region, and with $\Lambda > \lambda/n_I$ we have higher order diffracted modes in reflected region too. In this regime the contour maps became less ordered due to complex interaction between many modes. Finally, in between these two regions, when the wavelength is close to the grating period, we have dual-mode regime that is characteristic for HCG, with two waveguide-array modes inside grating and 0^{th} order diffracted mode outside the grating. In this region, large regions with high reflectivity are noticeable, and this is the region in which HCG is used as broadband reflector.

Optimum grating thickness for broadband reflectivity can be determined from the contour maps shown in Fig. 2.4. While high reflectivity regions do appear periodically with increasing



(a) (b)

Figure 2.4: Contour maps showing reflectivity of HCG versus normalized wavelength λ/Λ and grating thickness d/Λ for (a) TE-polarized and (b) TM-polarized incident plane wave. HCG parameters used for this simulation are $n_I = 1$, $n_{II} = 1.48$, $n_H = 3.48$, $n_L = 1$ and $f = 0.6$.

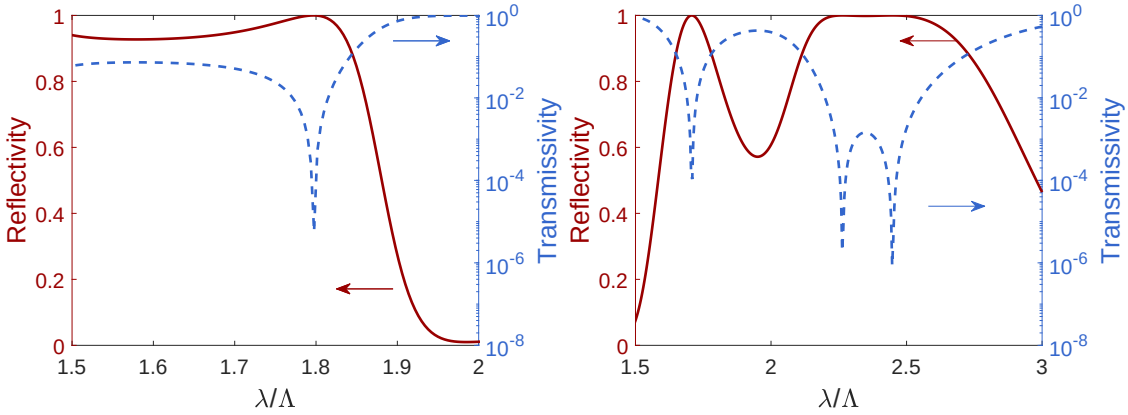


Figure 2.5: Reflectivity spectrums of the same HCG as in Fig. 2.4 for (a) TE HCG with $d/\Lambda = 0.376$ and (b) TM HCG with $d/\Lambda = 0.665$. Red solid line represents reflectivity in linear scale and blue dashed line represents transmissivity in log-scale.

thicknesses, the bandwidth is largest for the first such region, at smallest thickness. In this example, the broadest reflection bandwidth for TE HCG is achieved for thickness of $d = 0.376\Lambda$ and for TM HCG $d = 0.65\Lambda$, and reflection and transmission spectrums are shown in Fig. 2.5.

While TM HCG has larger thickness than TE HCG, it also shows much broader high reflectivity for filling factor of 0.6. Broader bandwidth could be achieved for TE polarization if filling factor is optimized too. Transmissivity spectrum is also shown in the same plots in logarithmic scale, and sharp dips in transmissivity are noticeable that correspond to GMR resonances or waveguide-array mode reflection points.

The polarization selectivity of HCG is more clearly illustrated on Fig. 2.6 where reflection spectrums for both polarizations are directly compared for identical design. HCG optimized to have high reflectivity at selected wavelength for TM-polarization will show low reflectivity for TE-polarization.

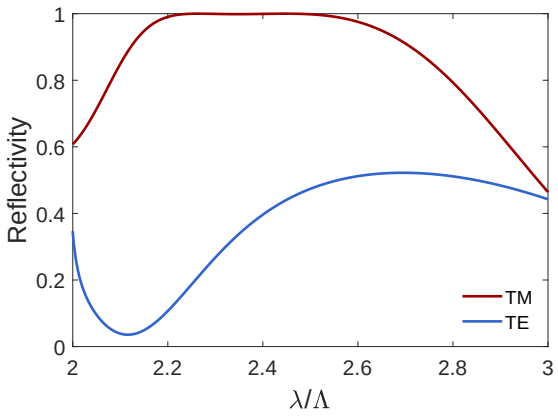


Figure 2.6: Comparison of reflectivity spectrums of the same HCG as in Fig. 2.4, with $d/\Lambda = 0.665$, for TM- and TE-polarization.

The results shown in this section are obtained using RCWA numerical simulation, which assumes an infinite periodic grating. However, in the real devices, the finite HCG size reduces the reflectivity that can be obtained [107]. As will be discussed later, this increases the threshold current and

reduces the energy efficiency of the lasers. This reduction in reflectivity can be attributed to losses via guided modes in the HCG excited due to the nonzero angular components in the finite-size incident wave [139].

HCG for TE and TM polarization

The polarization selectivity was previously discussed and illustrated. Comparing the grating parameters of the HCGs optimized for TE and TM polarization, several rules can be identified.

It was already pointed out that the optimum grating thickness for broadband reflectivity is smaller for TE polarization. The reason TE HCG can be thinner is due to larger effective refractive index for TE HCG [126]. Following the dual waveguide-array modes picture, it can be shown that high reflectivity is achieved when the phase difference between the two modes at the bottom interface plane is an odd integer multiple of π [119, 140]:

$$(k_{z,1} - k_{z,2})\mathrm{d} = \pi, \tag{2.13}$$

where $k_{z,1,2}$ are z-components of the wave vectors (propagation constants) of the waveguide-array modes. For both polarizations, mode 1 has more electric field confined within the grating bars, while mode 2 is more confined in the low refractive index between the bars [119]. As following from the boundary conditions, it can be determined that for TM mode 1 field is enhanced more in the low refractive-index region between the bars, while there is no enhancement for TE mode. Therefore, effective refractive index, which is obtained by averaging with the electric field as the weighing factor, is lower for TM mode 1 due to larger contribution of low refractive index. Since the propagation constants are proportional to effective refractive index, it follows that $(k_{z,1} - k_{z,2})$ is smaller for TM, which then means that grating thickness d must be higher [119].

Grating thickness is related to the period of the grating via wave vector [119]. The x-component of the wave vector is related to period, $k_x \sim 2\pi/\Lambda$, and $k_z \sim \pi/\mathrm{d}$ at high reflectivity condition. Then, following equation should be satisfied:

$$\left(\frac{2\pi}{\lambda}\right)^2 \sim \left(\frac{2\pi}{\Lambda}\right)^2 + \left(\frac{\pi}{\mathrm{d}}\right)^2. \tag{2.14}$$

Comparing TE and TM optimized HCGs, due to smaller thickness, TE HCG needs larger period Λ for high reflectivity at the set wavelength [119].

As explained before, HCG have only 0^{th} order diffraction modes propagating in the reflection and transmission regions. All other modes are evanescent. The z-component of the wave vectors of the evanescent modes is imaginary and it is given by Eq. (2.8):

$$k_{z,m} = -\mathrm{j}\sqrt{\left(\frac{2\pi m}{\Lambda}\right)^2 - \left(\frac{2\pi \mathrm{n}}{\lambda}\right)^2}, \tag{2.15}$$

where n is refractive index of the material outside of the grating. Following previous discussion, from Eq. (2.15), we can conclude that for TE HCG $k_{z,m}$ would be smaller, due to larger Λ. Therefore, the attenuation of evanescent modes is slower and field penetrates deeper into the low-refractive-index materials, compared to TM polarization. This evanescent tail plays a crucial role when designing the HCG reflectors, as the reflectivity can be reduced if the evanescent mode couples into another region with higher refractive index.

HCG heterostructure

When employed in vertical cavity, HCG reflector can be used for controlling the transverse optical confinement. By varying the grating parameters vertical-cavity in-plane heterostructure can be formed that can ensure confinement of the cavity mode [141]. This method can be alternative to index-guiding or shallow surface relief methods that are commonly used for optical mode confinement.

This is possible due to unique property of the HCG that it can modify the dispersion of the vertical cavity modes in the in-plane directions. The dispersion curvature is the second-order derivative of the frequency ω of a propagating mode with respect to the in-plane wave vector k. Total dispersion in the cavity has contributions from the two mirrors and the propagation in the cavity. In case of conventional cavities formed by DBR mirrors, dispersion is always positive for both DBRs and propagation. HCG can be engineered to have curvature that is either positive or negative, and can have a dominant contribution for total cavity dispersion [142]. It is anisotropic along the x- and y-directions and depends on the incident light polarization [143]. This properties gives great flexibilities to engineer HCGs to control the transverse mode sizes, wavelengths, and spatial orders separately in x and y directions [142–144].

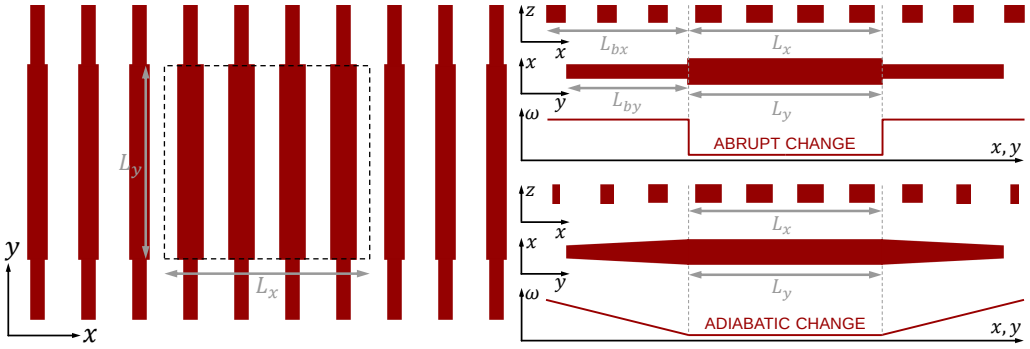


Figure 2.7: (a) Top schematic view of a HCG heterostructure showing the well with sizes L_x and L_y surrounded by barriers with different grating bar width. (b) Two types of barriers: abrupt and adiabatic. Cross-sectional view in x-z plane illustrates bar width change in x direction and top view in x-y plane illustrates bar width change in y direction.

An illustration of HCG heterostructure, in both x- and y-directions, is shown in Fig. 2.7a. By changing the grating parameters, dispersion curvature can be adjusted. Regions with different dispersion would have transverse modes at different wavelengths, forming a photonic barrier between them. By surrounding the central grating region with regions with different dispersion curvature, a photonic well can be formed in which transverse mode can be confined. The barrier length in the transverse directions should be larger several times than the barrier penetration depth in order to have an effective barrier and avoid lateral losses. The barrier height (in ω domain) should be short to avoid scattering losses that come from large perturbation, but reducing the height increases the penetration depth and therefore the mode size so the barrier height should be carefully optimized [145]. Another way to reduce the scattering losses is to change grating parameters adiabatically in the barrier regions as illustrated in Fig. 2.7b. With adiabatic change, higher Q-factors and lower lateral losses can be achieved [145].

HCG with In-Plane coupling

Another possibility that HCGs bring is in-plane light emission into a waveguide. If a waveguide is placed adjacent to the grating, a portion of the light that is incident in vertical direction can be coupled laterally into the waveguide. This property can be employed to integrate VCLs with silicon waveguides for on-chip lasers sources. Such devices have been investigated [60, 62] and demonstrated [63, 64].

In order to optimize coupling with the waveguide, the grating has to be carefully designed. The reflectivity should not drop fast with the incident angle. The cavity dispersion should be optimized, as it determines the lateral penetration, mode size and lateral light velocity [145]. Position of the waveguide to the cavity mode is also critical. The greater the overlap of the mode tail with the

waveguide, the better coupling can be achieved. If heterostructure is used, the barrier on the side on which the waveguide is should not be introduced.

2.2.3 Other applications of HCGs

HCG can be designed for a wide range of applications, other than as a reflector.

Since low-refractive-index material needs to surround the grating, HCGs are often realized as a membrane suspended in air. This enables the grating to be movable if nanoscale actuators are integrated. Such nanoelectromechanically movable HCG have been used to realize tunable lasers [113, 146] that showed much lower power consumption and much faster tuning speed compared to previous designs due to their smaller dimensions.

One application is as an optical resonator with an ultrahigh quality factor and surface-normal output coupling [127, 128]. In the reflectivity spectrum of this kind of HCG there is a very sharp change. The mechanism of these high Q-factor resonances can be explained in similar way as for conventional Fabry-Perot cavity, except now the two waveguide-array modes are together contributing to the resonance [147]. The resonance occurs when the grating thickness is such that a constructive interference is obtained at both top and bottom planes of the grating [140, 147].

HCGs have also been used to control the phase front of reflected and transmitted light and achieve focusing [148] or steering of the light [149]. These functionalities could replace the lenses and reduce optics packaging cost.

While polarization selectivity of the 1D-HCGs is useful for many application, polarization-independent 2D-HCGs have also been studied and demonstrated [150, 151].

2.3 Mirrors for VCSELs

Compared to the edge-emitting lasers, VCSELs have considerably smaller cavity volume. This is the key feature responsible for the three main advantages of VCSELs: lower threshold current (higher energy efficiency), higher relaxation resonance frequency (faster modulation) and larger free spectral range (single-mode operation) [152]. However, it also means that light is seeing much less gain during each round trip inside the cavity and many more round-trips are needed to achieve sufficient amplification. Therefore, mirrors that form the resonator for VCSELs need to have very high reflectance, usually higher than 99%, to reach the lasing threshold [153].

While some of earliest VCSELs used polished surfaces as mirrors, DBRs quickly became the main choice for VCSEL mirrors. Alternating quarter-wavelength layers of higher and lower refractive-index materials can produce very high reflectivity. The refractive-index contrast Δn and number of pairs N determine the reflectivity, however maximum possible reflectivity is limited by the absorption in the materials. The higher the Δn the less pairs it is needed to reach maximum reflectivity. Therefore, when choosing the materials for DBR stack, refractive-index contrast and material absorption are key properties [153].

Thermal properties of DBRs have great influence on the laser performance. Most often main heat sinking channels towards the substrate or heat sink structure go through the DBRs. This is of critical importance for InP-based lasers due to increased temperature dependent Auger recombination [153]. The multilayer stacks exhibit anisotropic thermal conductivity [154] which needs to be taken into account when modeling heat transfer of DBRs. In case of semiconductor DBRs, ternary and quaternary alloys have significantly lower thermal conductivities than binary alloys [155].

Low electrical resistance can be necessary in cases when the electrical contacts are formed on the DBRs. Doping of semiconductor mirrors increases the optical losses which limits the maximum reflectivity. Therefore, a compromise is necessary between optical losses and electrical resistance [153]. The p-type DBRs generally has higher resistance, and tunnel junctions are often necessary in order to avoid them.

2.3.1 Mirrors for LW-VCSELS

Epitaxially grown all-semiconductor Al(Ga)As/(Al)GaAs DBRs have enabled short-wavelength GaAs-based VCSELs with excellent performance [72]. Layers are relatively thin for short wavelengths, so the total thickness of these DBRs is not too large and, with good thermal conductivity of those alloys, good heat dissipation is ensured. Thanks to them, GaAs-based VCSELs have quickly advanced and AlGaAs/GaAs DBRs are standard even today. However, due to 3.7% lattice mismatch between GaAs and InP, they could not be directly employed for InP-based long wavelength lasers.

Epitaxial DBRs

Several material combinations for lattice matched, epitaxially grown, all-semiconductor DBRs in InP material system have been investigated and demonstrated [156]. Probably the most common one was based on InGaAsP/InP pairs [18, 157]. For this combination, Δn is limited to the range of 0.2 to 0.28, which is approximately half of Al(Ga)As/GaAs DBRs in GaAs-based system, and 40 to 50 pairs are needed for sufficient reflectivity. This makes this kind of mirrors significantly thicker. InGaAsP/InP DBRs have very poor thermal conductivity, so VCSELs with this kind of mirrors often cannot reach CW operation at room temperature [18]. InGaAlAs/InAlAs is one alternative lattice matched epitaxial mirror that has also been studied [91, 156, 158]. The Δn is close to InGaAsP/InP, but due to its use of ternary alloy instead of binary, the thermal conductivity is significantly worse. AlGaAsSb/AlAsSb lattice matched combination has the Δn around 0.4–0.54, and 20–30 pairs is sufficient for high reflectivity, but they too suffer from low thermal conductivity [89].

As none epitaxial DBRs lattice matched to InP could provide good enough properties, a lot of effort was done to bring Al(Ga)As/GaAs DBRs to InP-based VCSELs. This has been done in two ways: using wafer fusion [159] and metamorphic growth [160]. With metamorphic growth, the lattice-matching constrain can be avoided, however additional buffer layer is needed to prevent dislocation propagation. With wafer fusion, the Al(Ga)As mirrors are grown on GaAs substrates and active layer is grown on InP substrate. Active epitaxy is joined first with one mirror using wafer fusion, which is done at temperatures above 600°C in vacuum or hydrogen atmosphere and with enormous pressure applied for about 30 minutes, which causes wafers to undergo a slight plastic deformation resulting in a uniform contact on a nanometer scale and covalent bonds are formed between wafers. Then the InP substrate can be removed and same method can be applied again for second mirror. Long wavelength VCSELs based on wafer fused Al(Ga)As/GaAs DBRs have been successfully demonstrated with performance superior to those with InP-based DBRs [103, 161, 162]. With relatively high Δn around 0.48 for AlAs/GaAs and 0.33 for AlGaAs/GaAs, sufficient reflectivity can be reached with 20 to 30 pairs. AlAs is often preferred in bottom DBR since it has one order of magnitude higher thermal conductivity compared to AlGaAs. However, unproven reliability of such lasers and very high cost, due to large waste of expensive III-V material, are main drawbacks of this method.

Dielectric DBRs

Alternative to semiconductor epitaxial mirrors is to use deposited or sputtered dielectric materials to form a DBR [153]. Since there is no lattice-matching condition, material choices are limited only by absorption at targeted wavelength. Therefore, DBR can be formed with material combination with much higher Δn, and the maximum reflectivity can be reached with very few pairs. While this presents a great advantage for thin mirrors, use of dielectric materials means that current injection cannot be done through the DBRs, so intra-cavity contact scheme must be used. Furthermore, dielectric materials most often have low thermal conductivities. They are often employed on *p*-side of the laser to avoid poor *p*-type epitaxial DBRs [18, 157], although double dielectric DBR cavities have also been used [95, 163]. Most commonly used dielectric DBR are SiO_2/*a*-Si [157, 163]. With Δn around 2.2, high reflectivity can be reached with as few as 4 pairs, but is limited by absorption in *a*-Si. Al_2O_3/*a*-Si offers improved thermal conductivity, comparable to AlAs/GaAs,

but has somewhat lower Δn around 1.9 [18, 163]. TiO_2 can be used instead of *a*-Si to lower the absorption [158]. CaF_2-based mirrors, such as CaF_2/*a*-Si with $\Delta n = 2.2$ and CaF_2/ZnS with $\Delta n = 0.95$, have also been used [95]. Often, on non-emitting side, a layer of metal can be deposited to act as an additional reflector so the number of DBR pairs can be reduced even further [95, 158, 163]. Such hybrid mirrors also improve the thermal properties of the device with meal acting as heatsink.

HCG as VCSEL mirror

Finally, as introduced and reviewed in the Introduction chapter, HCGs have been employed successfully as an alternative to conventional DBR as a mirror for VCSELs. The many features of HCGs have been discussed and explained in previous section. The reflective bandwidth can be much higher than the epitaxial DBRs and comparable with dielectric DBRs. HCGs have been demonstrated using various materials such as GaAs [57], InP [58, 112] and Si [59, 60, 64], surrounded by air or SiO_2 as low-refractive-index material.

Comparison of LW-VCSEL mirrors

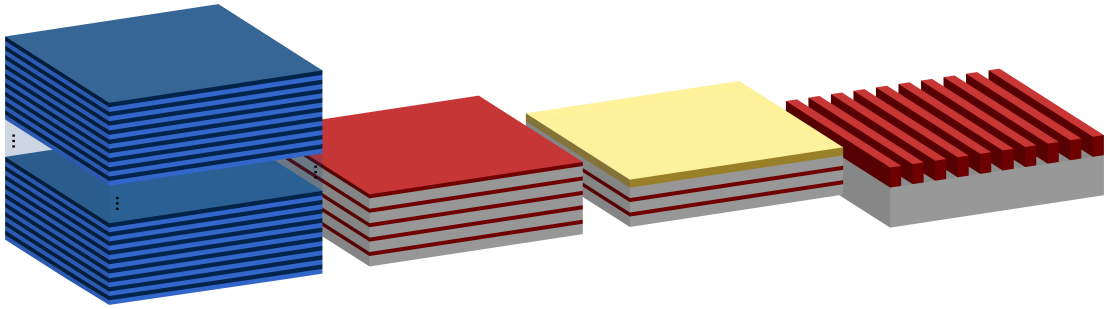


Figure 2.8: Schematic illustrations of mirrors for VCSELs. From left to right: epitaxial DBR, dielectric DBR, hybrid dielectric DBR and HCG.

Four of the discussed different mirror types are illustrated on Fig. 2.8, comparing their relative thickness. With epitaxial DBR, despite each layer thickness is relatively small, several tens of pairs are needed to reach the needed reflectivity, so their thickness can be as much as 10 μm. Dielectric DBR, often have one layer of the pair with very low refractive index, so those layers may be relatively thicker, but with only 4–6 needed pairs, their total thickness can be 1–3 μm. Hybrid mirrors are even thinner, if the metal layer thickness is not accounted for. With HCGs, the trend of reducing the mirror total thickness is pushed even further. The grating layer can be thinner than 500 nm, about half of thinnest dielectric DBRs, if surrounded by sufficiently thick low-refractive-index material.

In order to compare these mirrors, looking at the thickness only is not enough. A figure of merit used to characterize the reflection is fractional bandwidth (FB), which can be defined as ratio of 99% reflectivity frequency bandwidth and central frequency [164]:

$$\mathrm{FB} = \frac{\Delta\omega}{\omega_0}. \tag{2.16}$$

While FB can be used to compare bandwidth of different mirrors, it doesn't take into the account the thickness of the mirror. Therefore, another figure of merit can be defined as bandwidth over thickness (BOT):

$$\mathrm{BOT} = \frac{\Delta\lambda}{\mathrm{d}}, \tag{2.17}$$

where $\Delta\lambda$ is again 99% reflectivity wavelength bandwidth and d is mirror thickness.

Table 2.1: FB and BOT for epitaxial DBR, dielectric DBR and TM HCG shown in Fig. 2.9.

Type	Materials	Pairs	Δn	Thickness (μm)	FB (%)	BOT (%)
Epitaxial DBR	AlAs/GaAs	30	0.49	7.64	9.46	1.97
Dielectric DBR	SiO_2/a-Si	5	2.15	1.87	51.6	45.8
TM HCG	air/Si	1	2.48	0.45	14.3	48

Examples of reflectivity spectrums of three most successful mirrors for 1550 nm VCSELs, epitaxial wafer-fused AlAs/GaAs DBR, SiO_2/a-Si dielectric DBR deposited and air/Si TM-optimized HCG, are shown in Fig. 2.9. Reflectivity has been calculated numerically using RCWA

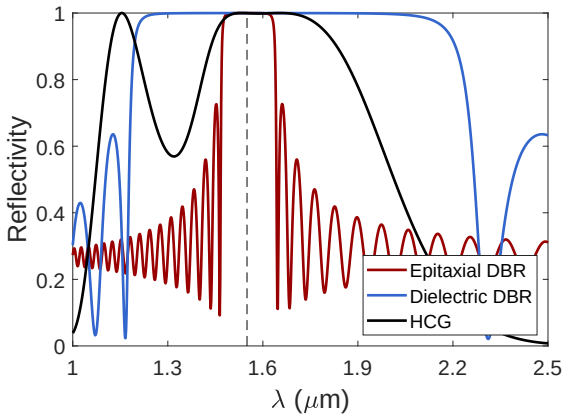


Figure 2.9: Reflectivity spectrum of three different mirrors. The parameter of each structure are given in Table 2.1. The dashed black line represents the targeted wavelength of each mirror, which is 1.55 μm in this example.

and refractive index values for materials are taken from [153]. Incident medium for DBRs is assumed to be InP and number of pairs used is sufficient for very high reflectivity. For HCG, the incident medium is air and the low-refractive-index material below the grating is SiO_2, and filling factor is f = 0.6. For simplicity, dispersion and absorption have not been considered. The Table 2.1 lists the resulting FB and BOT values. It is clear that even best epitaxial DBR has significantly lower FB than both dielectric DBR and HCG. Dielectric DBR dominates with largest bandwidth. However, looking at the BOT we can see that HCG offers best tradeoff.

2.3.2 Phase and energy penetration depth

High and broadband reflectivity of the mirrors is important for reaching the lasing threshold, and materials properties and physical mirror thickness are important for fabrication and thermal properties of the lasers, but there is more to mirror design than that. Reflection phase is related to resonant wavelength of the cavity and penetration of mode energy determines the mode confinement and directly influences the modulation speed of the laser.

Lasing condition

A schematic illustration of the simple conventional VCSEL structure is shown in Fig. 2.10. The light is traveling in vertical z-direction, passing through the active and passive regions and reflecting between top and bottom mirror that form the Fabry–Pérot (FP) cavity.

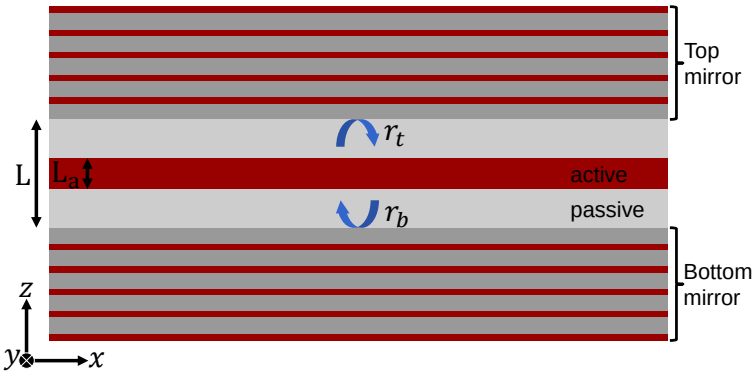


Figure 2.10: Schematic illustration of basic VCSEL structure, comprised of two mirrors and optical cavity which contains active and passive regions.

The time- and space-varying electric field of the lasing mode in the cavity, assuming TE polarization, can be written as [123]

$$E_y = \hat{y} E_0 U(x,y) \mathrm{e}^{\mathrm{j}(\omega t - \tilde{\beta} z)}, \tag{2.18}$$

where $\hat{y}$ is unit vector, E_0 is the magnitude of the field and $U(x,y)$ is normalized transverse electric field profile. This mode propagates in the z direction as $e^{-\mathrm{j}\tilde{\beta}z}$, where the complex propagation constant $\tilde{\beta}$ includes any loss or gain. The complex propagation constant can be expressed as

$$\tilde{\beta} = \beta + \frac{\mathrm{j}}{2}(\Gamma_{xy} g - \alpha_i), \tag{2.19}$$

where $\beta = 2\pi \bar{\mathrm{n}}/\lambda$ is real propagation constant, $\Gamma_{xy} g$ is modal gain and α_i is internal modal loss. $\bar{\mathrm{n}}$ is effective refractive index and Γ_{xy} is transverse confinement factor. As the gain is present only in active region of the cavity and the losses can be significantly different in active and passive regions, complex propagation constant for active and passive regions, respectively, are

$$\tilde{\beta}_{\mathrm{a}} = \beta_{\mathrm{a}} + \frac{\mathrm{j}}{2}(\Gamma_{xy} g - \alpha_{i,\mathrm{a}}), \tag{2.20a}$$

$$\tilde{\beta}_{\mathrm{p}} = \beta_{\mathrm{p}} + \frac{\mathrm{j}}{2}(-\alpha_{i,\mathrm{p}}). \tag{2.20b}$$

Mirror losses and reflection phase change are described by complex amplitude reflection coefficients [123]:

$$r_{\mathrm{t}} = |r_{\mathrm{t}}| e^{-\mathrm{j}\phi_{\mathrm{t}}}, \tag{2.21a}$$

$$r_{\mathrm{b}} = |r_{\mathrm{b}}| e^{-\mathrm{j}\phi_{\mathrm{b}}}, \tag{2.21b}$$

where r_{t} and r_{t} are the complex mirror reflection coefficients for the top and bottom mirrors, respectively, $|r_{\mathrm{t}}|$ and $|r_{\mathrm{b}}|$ account for the losses of the light that penetrates the mirror as well as losses due to non-unit reflection, and the corresponding phase terms are ϕ_{t} and ϕ_{b}.

The lasing threshold is reached when during one round trip all the propagation and mirror losses are compensated by the gain and the total phase change of the field is integer multiple of 2π for constructive interference. The lasing condition can be written in following form [123]:

$$r_{\mathrm{t}} r_{\mathrm{b}} \mathrm{e}^{-\mathrm{j}2\tilde{\beta}_{\mathrm{a,th}} \mathrm{L_a}} \mathrm{e}^{-\mathrm{j}2\tilde{\beta}_{\mathrm{p,th}} \mathrm{L_p}} = 1, \tag{2.22}$$

where complex propagation constants are at threshold values, and $\mathrm{L_a}$ and $\mathrm{L_p} = \mathrm{L} - \mathrm{L_a}$ are lengths of active and passive region, as depicted on Fig. 2.10. The lasing condition can be separated into

two conditions: for amplitude and phase. By inserting Eqs. (2.20) and Eqs. (2.21) into Eq. (2.22), the amplitude condition is obtained as

$$|r_{\mathrm{t}}||r_{\mathrm{b}}|\mathrm{e}^{(\Gamma_{xy}g_{\mathrm{th}}-\alpha_{i,\mathrm{a}})\mathrm{L_a}}\mathrm{e}^{-\alpha_{i,\mathrm{p}}\mathrm{L_p}}=1. \tag{2.23}$$

By taking the phase of the left term in Eq. (2.22) and set it to integer multiple of 2π, the phase condition is obtained as:

$$\phi_{\mathrm{t}}+\phi_{\mathrm{b}}+2\beta_{\mathrm{a,th}}\mathrm{L_a}+2\beta_{\mathrm{p,th}}\mathrm{L_p}=2m\pi,\quad m=1,2,\cdots. \tag{2.24}$$

In a more general case, a cavity could be comprised of multiple different layers, and contributions of all layers would be added up, so the amplitude and phase conditions would become

$$|r_{\mathrm{t}}||r_{\mathrm{b}}|\mathrm{e}^{\Gamma_{xy}g_{\mathrm{th}}\mathrm{L_a}}\mathrm{e}^{-\sum_k\alpha_{i,k}\mathrm{L_k}}=1, \tag{2.25}$$

$$\phi_t+\phi_b+2\sum_k\beta_{k,\mathrm{th}}\mathrm{L}_k=2m\pi,\quad m=1,2,\cdots, \tag{2.26}$$

where $\alpha_{i,k}$ and L_k are loss term and thickness of each layer and summation also includes active layer $\mathrm{L}_k=\mathrm{L_a}$. The amplitude condition determines the threshold gain needed for lasing, and phase condition determines the lasing wavelength.

Effective mirror and phase penetration

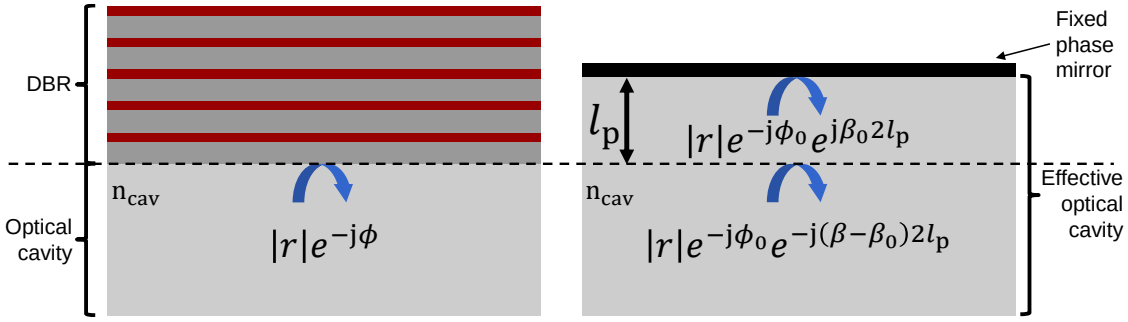


Figure 2.11: Illustration of effective mirror concept. On the left is a linear phase mirror and on the right is equivalent fixed phase mirror displaced by length l_p.

With the DBR, light is not reflected instantaneously, but gradually as it propagates through the stack. This can be approximated by a discrete mirror with fixed reflection phase displaced by the penetration depth l_p, as illustrated in Fig. 2.11. The reflection phase of DBR is approximately linear around the Bragg frequency in the region of high reflection, as can be seen from the examples shown in Fig. 2.12, so the phase can be expanded in a Taylor series around Bragg frequency:

$$\phi\approx\phi_0+(\beta-\beta_0)\frac{\partial\phi}{\partial\beta}\bigg|_{\beta=\beta_0}+\cdots, \tag{2.27}$$

where ϕ_0 is the phase change at the Bragg frequency, which is 0 or π depending on a refractive index of the incident medium, and $\beta_0=\mathrm{n_{cav}}\omega_0/c$ is propagation constant at Bragg frequency ω_0 for which the DBR is designed. If we keep only first linear part, we can express reflection coefficients as [123]

$$r\approx|r|e^{-\mathrm{j}\phi_0}\mathrm{e}^{-\mathrm{j}(\beta-\beta_0)2l_\mathrm{p}}, \tag{2.28}$$

where l_p is penetration depth given by

$$l_\mathrm{p}\equiv-\frac{1}{2}\frac{\partial\phi}{\partial\beta}\bigg|_{\beta=\beta_0}, \tag{2.29}$$

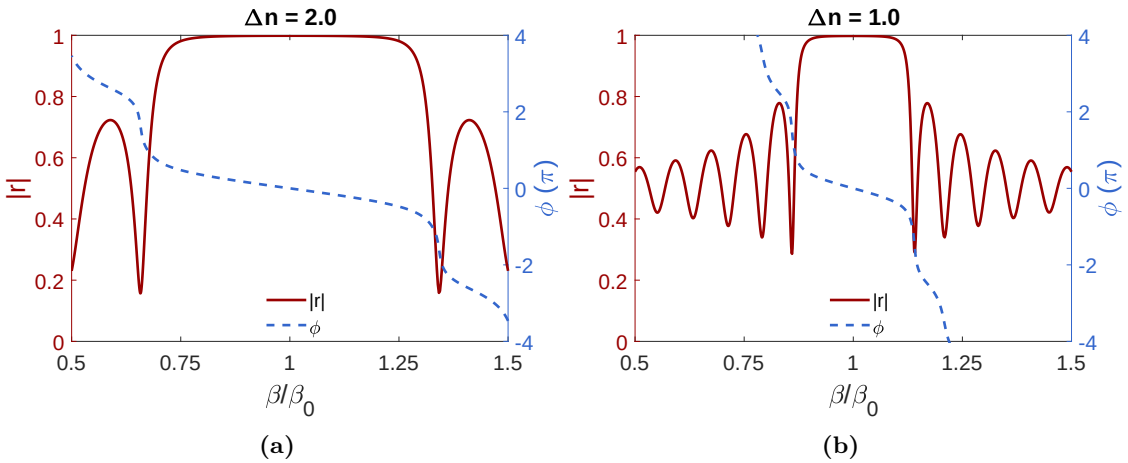


Figure 2.12: Calculated amplitude and phase of the reflection on the DBR structures consisting of (a) 5 pairs with $\Delta n = 2$ and (b) 12 pairs with $\Delta n = 1$ The incident medium is InP, and air is on the opposite side.

and factor of 2 is accounting for a round trip back to reference plane. The fixed mirror reflection phase is equal to the phase reflection at the Bragg frequency: $\theta = 2l_p\beta_0 = \omega_0\tau$, where τ is reflection time delay that can be defined as the time which light takes to travel the penetration depth, and can be obtained as [164, 165]:

$$\tau = -\frac{\partial\phi(\omega)}{\partial\omega}\bigg|_{\omega=\omega_0} = -\frac{n_{cav}}{c}\frac{\partial\phi(\omega)}{\partial\beta}\bigg|_{\beta=\beta_0}, \tag{2.30}$$

where ω is the angular frequency of the incident light. The time delay of the mirror needs to be considered when investigating the photon lifetime of the cavity.

The time delay and penetration depth have been calculated for the DBR example shown in Fig. 2.12a, which has 5 pairs of layers with refractive indices of $n_{high} = 3.5$ and $n_{low} = 1.5$. The total DBR thickness at 1.55 μm is close to 2 μm, but the phase penetration is around 193 nm and the time delay around 4 fs, showing that reflection reaches its maximum very quickly. As the Δn of the DBR reduces, the high reflection region becomes narrower and phase change becomes steeper, so the penetration depth and time delay increase. For DBR example shown in Fig. 2.12b, refractive indices are $n_{high} = 3.5$ and $n_{low} = 2.5$, so the total DBR thickness is around 3.2 μm, but the penetration depth and the time delay are doubled to 386 nm and 8 fs, respectively.

The reflection phase of the HCGs is also approximately linear in the high reflection region. So the same phase penetration and effective mirror concept can also be applied for HCG [166].

If we use the effective mirror concept and insert Eq. (2.28) into Eq. (2.26), the phase condition can be written as

$$(\phi_{0,t} + 2l_{p,t}\beta_{t,th} - \theta_{0,t}) + (\phi_{0,b} + 2l_{p,b}\beta_{b,th} - \theta_{0,b}) + 2\sum_k \beta_{k,th}L_k = 2m\pi, \quad m = 1, 2, \cdots, \tag{2.31}$$

which can be rewritten in terms of lasing wavelength λ_{th} in following way:

$$(\phi_{0,t} + \phi_{0,b} - \theta_{0,t} - \theta_{0,t}) + \frac{4\pi}{\lambda_{th}}(l_{p,t}n_{cav,t} + l_{p,b}n_{cav,b} + \sum_k n_{cav,k}L_k) = 2m\pi, \quad m = 1, 2, \cdots, \tag{2.32}$$

where $n_{cav,t}$ and $n_{cav,b}$ are refractive indices of the effective cavity for top and bottom mirror, respectively. We can see that mirrors penetration depths play important role in determining the lasing wavelength. The poorer the mirror and steeper the phase slope, the larger influence of the mirror on the lasing wavelength is. This can be undesirable if the gain spectrum is narrow and

precise control of the wavelength is needed, but it can also be beneficial, e.g., for tunable lasers. Usually, for VCSELs with two DBRs, the target wavelength is designed to be same as Bragg wavelength of the mirrors, and in that case the contribution from phase penetration is annulled from the phase condition and only ϕ_0 terms are left. If the refractive index in cavity is higher than the refractive index of first mirror layer, the ϕ_0 is equal to 0 for TE polarization, and phase condition is only determined by the optical cavity:

$$2\sum_k \beta_{k,\mathrm{th}} \mathrm{L}_k = 2m\pi, \quad m = 1, 2, \cdots . \tag{2.33}$$

Energy penetration and confinement factor

Another characteristic length that can be defined for mirrors is energy penetration depth, used to describe how deep does the optical energy of the mode effectively extend into the mirror [105, 164, 165]. Energy and phase penetration depth are often assumed to be equal, but that is not always the case, especially with mirrors that are not DBRs. A general way to define the energy penetration depth is the length at which the intensity decreases to 1/e of incident intensity.

For DBR, the energy penetration depth can be estimated using simple analytic expression [123]:

$$l_\mathrm{e} = \frac{m_\mathrm{eff}}{2}\Lambda, \tag{2.34}$$

where Λ is the period of the stack equal to sum of two quarter wavelength layer thicknesses, and m_eff is effective number of periods given by

$$m_\mathrm{eff} = \frac{\tanh(2m\bar{\mathrm{r}})}{2\bar{\mathrm{r}}}, \quad \bar{\mathrm{r}} = \frac{\mathrm{n_H} - \mathrm{n_L}}{\mathrm{n_H} + \mathrm{n_L}}, \tag{2.35}$$

where m is total number of periods. The total energy that penetrates into the mirror can be estimated as if the energy density at the input extends into the mirror by l_e. In general, the energy penetration depth is larger than phase penetration depth, and for small refractive-index contrast the energy distribution is close to uniform and l_e gets close to DBR thickness [164].

For some mirror types, like photonic crystal mirrors or HCGs, the reflection mechanism is different, light is also guided in lateral direction and often enhanced within the mirror. So it is difficult to derive an analytical expression for penetration depth or determine it as intensity decrease of $1/e$. In these cases, the energy penetration depth is often investigated numerically [165] or estimated from the transmission or reflection as [105]

$$T = 1 - R = \mathrm{e}^{-\mathrm{d}/l_\mathrm{e}}, \tag{2.36}$$

where T is transmittance, R is reflectance and d is mirror total thickness. For HCG, this expression may not be accurate, since it doesn't take into the account the extended evanescent tail of the field in low-refractive-index material beneath the grating. This tail can be significantly different for different polarizations. Therefore, the energy penetration depth is most accurately found from numerical simulations. In general, HCGs show significantly shorter penetration depth compared with traditional DBRs.

The energy penetration depth quantifies how optical energy is extending into the mirrors of the laser, so it plays the role in determining the effective mode volume and confinement factor [167]. The effective cavity length can be defined to account for both the cavity length and the mirror penetration. It can be simply estimated by

$$\mathrm{L_{eff}} = \mathrm{L} + l_\mathrm{e,t} + l_\mathrm{e,b}, \tag{2.37}$$

where L is the length of the cavity between the mirrors, and $l_\mathrm{e,t}$ and $l_\mathrm{e,b}$ are energy penetration depths of top and bottom mirror, respectively.

As the gain is not uniformly present inside the cavity, but only in limited active region, to determine the net effect of gain on the light, a weighted average of the gain distribution must be

taken across the total cavity. The averaged gain is called modal gain and, in most general case, the averaging can be done using electric field distribution in following way [123]:

$$\langle g \rangle = \frac{\int E^*(x,y,z) g(x,y,z) E(x,y,z)\,\mathrm{d}V}{\int |E(x,y,z)|^2\,\mathrm{d}V}, \tag{2.38}$$

where integration is done across the whole volume V of the laser, including mirrors. If the gain is assumed to be uniform inside the active region and zero outside it, it can come out of the integral but the integration boundary in nominator is only the active region, while in denominator the integration extends across whole cavity:

$$\langle g \rangle = g \frac{\int\limits_{V_\mathrm{a}} |E(x,y,z)|^2\,\mathrm{d}V}{\int\limits_{V} |E(x,y,z)|^2\,\mathrm{d}V} \equiv \Gamma g, \tag{2.39}$$

where Γ is called cavity confinement factor. The integration across different dimensions can be separated in most cases, with in-plane field distribution giving transverse confinement factor Γ_{xy}, and longitudinal field distribution giving longitudinal confinement factor Γ_z, so that $\Gamma = \Gamma_{xy}\Gamma_z$. The longitudinal confinement factor can then be approximated using [168, 169]

$$\Gamma_z = \frac{\int\limits_{\mathrm{L_a}} |E(z)|^2\,\mathrm{d}z}{\int\limits_{\mathrm{L}} |E(z)|^2\,\mathrm{d}z}. \tag{2.40}$$

In simplest case, assuming sinusoidal standing wave of the electric field, the longitudinal confinement factor becomes [123, 168]:

$$\Gamma_z = \frac{\mathrm{L_a}}{\mathrm{L_{eff}}} \left(1 + \frac{\sin(\mathrm{k_a L_a})}{\mathrm{k_a L_a}}\right), \tag{2.41}$$

where $\mathrm{k_a}$ is the propagation constant in the active region, and $\mathrm{L_{eff}}$ is result of integration in denominator. Γ_z is often approximated to be just $\mathrm{L_a/L_{eff}}$, however the enhancement factor given in the brackets becomes relevant when $\mathrm{L_a}$ becomes comparable to or smaller than λ, which is exactly the case for VCSELs. If the mode intensity peak overlaps well with active region, the longitudinal confinement factor can become close to $\Gamma_z = 2\mathrm{L_a/L_{eff}}$.

The effective cavity length, that includes energy penetration depth of the mirrors, is a crucial parameter for increasing the longitudinal confinement factor which would lower the lasing threshold, improve efficiency, and also improve modulation response.

2.3.3 Comparison of TE and TM HCG designs

HCGs are considered as very compact mirror alternative for DBRs. While the thickness of the grating itself is certainly small, it should not be forgotten that it needs to be surrounded by a low-refractive-index material in both reflection and transmission region. When HCG is used as a mirror for lasers, the reflection region is part of the optical cavity, and as such its thickness accounts to the cavity length and needs to be carefully optimized. In practical realizations where HCG has been used as a top mirror [57, 112], the transmission region is most often just free space above the device and there are no restrictions or issues. However, if used as a bottom mirror in hybrid III-V-on-Si approaches [59, 60, 64], where transmission region is the buried oxide (BOX) layer of the SOI substrate, thickness is limited by the practical thickness of the BOX layer.

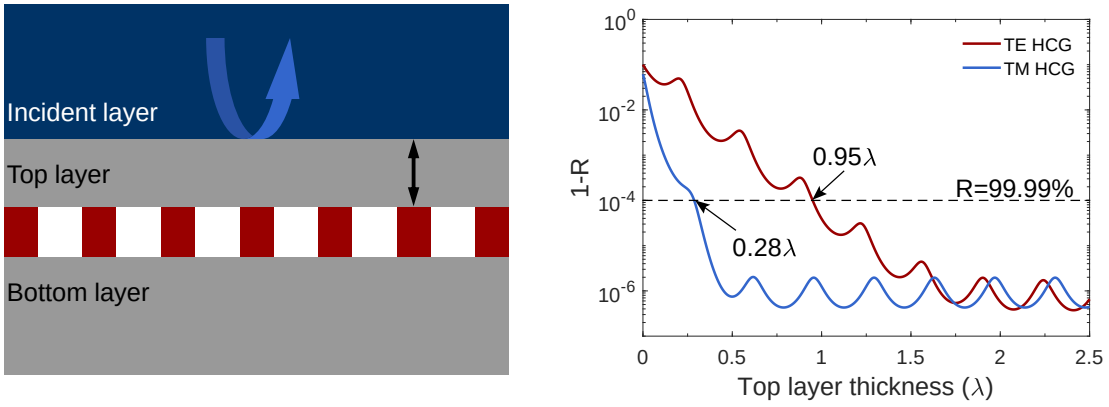
Table 2.2: Geometrical grating parameters TE and TM HCG optimized for $\lambda = 1.55\,\mu$m.

Polarization	d (nm)	Λ (nm)	f	fΛ (nm)
TE	245	980	0.311	305
TM	480	675	0.51	344

Therefore, low-refractive-index regions need to be taken into account when HCGs are employed in laser cavities.

In the section about HCGs, the differences in design of TE- and TM-optimized gratings were explained. It was shown that TE HCGs have smaller thickness and larger period when optimized for broadband high reflectivity around set wavelength, compared to TM HCGs. As a consequence, TE HCGs also have longer evanescent tail in the low-refractive-index regions. If the evanescent field reaches a high-refractive-index region, it may start propagating again causing leaking of optical power and reduction of the reflectivity. Here the constrains for thicknesses of low-refractive-index layers are investigated and compared for TE- and TM-HCGs.

The low-refractive-index material in reflection region is part of the cavity, so its exact thickness is dictated by the phase condition. However, the minimal thickness is determined by the length of the evanescent tail and the minimum reflectivity that is necessary. If the thickness is not large enough, the evanescent tail will couple to the high-refractive-index layer of the III-V epitaxy and reflectivity will be reduced. The lower reflectivity means higher mirror losses, which causes the rise in the threshold. In order to investigate this effect and compare the two polarizations, a numerical study was performed. The schematic of the structure that was simulated is shown on Fig. 2.13a. In this example, the HCG consist of Si ($n_H = 3.48$) grating bars with air ($n_L = 1$) between them, and SiO_2 ($n_{I,II} = 1.48$) layer surrounding it. HCG is imagined as a bottom mirror in a cavity, so the SiO_2 layer in reflection region is named top layer, while SiO_2 layer in transmission region is named bottom layer. The exact grating parameters for HCG optimized for maximum reflection at $\lambda = 1.55\,\mu$m for both polarizations are given in Table 2.2. The incident light comes from the top, and the material of half-infinite incident layer is taken to be InP ($n_{InP} = 3.1661$). The bottom layer is assumed to be half-infinite. The RCWA simulations are done for varying thickness of the top layer, and drop in reflectivity $(1 - R)$ is plotted as a function of the top layer thickness in



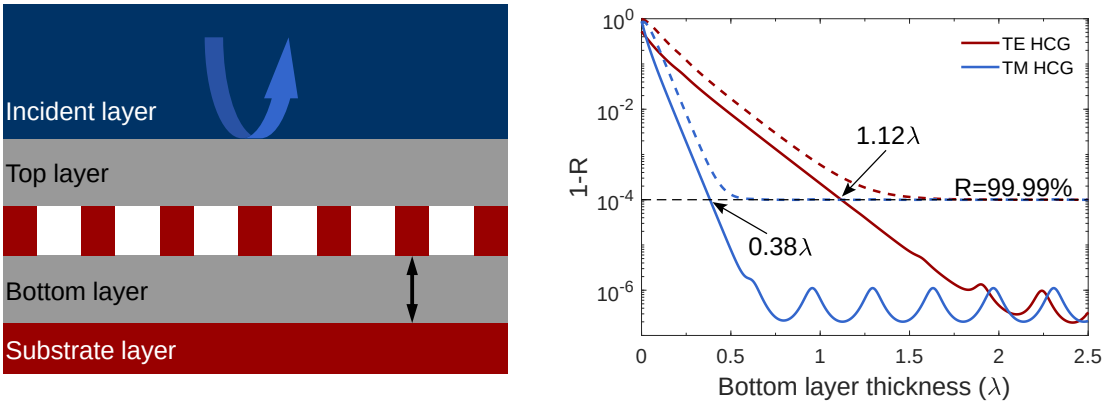
(a) **(b)**

Figure 2.13: (a) The schematic of the HCG structure. The blue arrow represents the incident light. (b) The reflectivity reduction as seen from the incident layer as a function of top layer thickness for TE and TM HCG. The y-axis is represented in log-scale. The x-axis is normalized to wavelength. Black dashed line represents the 99.99% threshold.

Fig. 2.13b. The gratings have been optimized so that minimum $1-R$ is below 10^{-6} for sufficiently large top layer thickness. As the thickness is reduced, the reflectivity drop starts to rise sooner for TE HCG than for TM HCG. If 99.99% reflectivity is set as a reference level, for this example the TM HCG reaches this value at top layer thickness of 0.28λ, while TE HCG requires 0.95λ, about 3.4 times thicker. If the top layer is chosen to be air, then the evanescent tail will be shorter, and layers as thin as 0.1λ can guarantee 99.99% reflectivity for TM HCG [120]. This can be shorter than a single layer of dielectric DBRs.

Shorter top layer thickness is advantageous as it enables shorter cavities and better heat dissipation. While use of materials like SiO_2 over air increases this thickness, they offer better thermal properties, easier fabrication and better reliability. Counting both minimum top layer thicknesses and the thickness of the grating itself, in this example, TM HCG would have total thickness of around 0.59λ (around 915 nm for $\lambda = 1.55\,\mu$m). For TE HCG, total thickness is around 1.11λ ($1.72\,\mu$m for $\lambda = 1.55\,\mu$m). While the grating itself can be half the thickness of TM HCG, more than 3 times higher top layer thickness makes TE HCG effectively twice as thick as TM HCG, and comparable with the thickness of dielectric DBR. 99.99% is rather strict condition, and in practice even lower reflectivities could be good enough, so the thickness of the top layer can be even shorter.

The thickness of the bottom layer needs to be considered if the HCG is used as a bottom mirror of the VCSEL, since the evanescent tail can couple to the high-refractive-index layer of the substrate. In order to investigate this effect, similar structure as in the previous case is simulated, except the bottom layer has finite thickness and half-infinite Si substrate layer is added below it, as illustrated on Fig. 2.14a. Now the bottom layer thickness is varied and reflectivity reduction is plotted on Fig. 2.14b. Two cases have been investigated. In first case, top layer thickness is set to 2λ which is high enough for maximum reflectivity. The reflectivity drops below 99.99% for bottom layer thickness below 0.38λ and 1.12λ for TM and TE HCG, respectively. In the second case, the top layer thickness is chosen for exactly 99.99% reflectivity. In this case, the reflectivity starts to drop around 0.6λ for TM and 1.8λ for TE HCG, which is exactly the point at which $1-R$ starts to rise for previous case. Again, the advantage of TM HCG design is clear. The second case represents the much tougher criteria, and it illustrates the combined effect of reflectivity drop



(a) **(b)**

Figure 2.14: (a) The schematic of the HCG structure with substrate layer added. The blue arrow represents the incident light. (b) The reflectivity reduction as seen from the incident layer as a function of bottom layer thickness for TE and TM HCG. The y-axis is represented in log-scale. The x-axis is normalized to wavelength. Black dashed line represents the 99.99% threshold. Full lines are obtained for large top layer thickness for maximum reflectivity, and dashed lines are obtained for top layer thickness optimized for 99.99% reflectivity.

from both layers. Usually, the top layer is more critical and should be minimized, while practical restrains on bottom layer are less strict.

Thinner bottom layer is advantageous for better heat dissipation. Low refractive index material, such as SiO_2 of the BOX layer, have low thermal conductivity, and represents an obstacle for heat flow towards the substrate. Therefore, by reducing this layer thickness as much as possible, thermal properties of the device can be improved.

2.4 Designing a high-speed VCSEL

In order to understand how to push the high-speed performance of the VCSELs, it is necessary to first understand what fundamentally determines the dynamic behavior of the lasers and to find out how the design limits the bandwidth.

The dynamic behavior can be, in a simple way, deduced by studying the modulation transfer function, which describes the response of the device to modulated input. For lasers, this modulation response is comprised of two parts: the intrinsic laser response of the optical output to current modulation, and extrinsic parasitic response of the electrical elements of the laser. The cascaded two-port model of the laser can be used to separates the two parts and enables them to be considered separately [170]. The overall modulation frequency response can then be written as

$$H(f) = \left| H_{\text{int}}(f) \cdot H_{\text{par}}(f) \right|^2, \tag{2.42}$$

where H_{int} is intrinsic response and H_{par} is parasitic response.

In this section, the intrinsic modulation response H_{int} is considered in effort to identify what design parameters influence the bandwidth and to gain insight into how can it be improved. The parasitic response will be considered in next chapter.

2.4.1 Intrinsic modulation response

The dynamic behavior of the interaction between photons and carriers in semiconductor laser is commonly described by rate equations [123, 167]. The rate equations are coupled set of equations for carrier density and photon densities for each laser mode. In the following analysis, single transverse mode emission is assumed, so that only one photon density equation is considered, which has been shown to be good enough approximation even for multimode VCSELs with highly overlapping transverse fields (such as index guided VCSELs) [171].

Rate equations

In their simplest form the rate equations can be written as [123]

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \frac{\eta_i I}{q \mathrm{V_a}} - \frac{N}{\tau} - v_{\mathrm{g}} g N_p, \tag{2.43a}$$

$$\frac{\mathrm{d}N_p}{\mathrm{d}t} = v_{\mathrm{g}} \Gamma g N_p + \Gamma \beta_{\mathrm{sp}} R_{\mathrm{sp}} - \frac{N_p}{\tau_p}, \tag{2.43b}$$

where N is the carrier density, N_p is the photon density. The carrier density is increased by generation of carriers due to current I in the active volume $\mathrm{V_a}$ with injection efficiency η_i, and is decreased by carrier decay and stimulated emission. The carrier decay is determined by carrier lifetime τ and takes into account the spontaneous emission, leakage rate and non-radiative recombination. The stimulated emission is determined by photon density, gain g and group velocity v_{g}. The photon density is increased by stimulated emission factored by confinement factor Γ as well as spontaneous emission R_{sp} portion that couples into the lasing mode described by spontaneous emission factor β_{sp}. The photon density is decreased by photon decay, determined by the photon lifetime τ_p.

The gain can be well approximated by four-parameter logarithmic formula [123]:

$$g(N, N_p) = \frac{g_0}{1 + \varepsilon N_P} \ln\left(\frac{N + N_\mathrm{s}}{N_\mathrm{tr} + N_\mathrm{s}}\right), \tag{2.44}$$

where g_0 is the gain coefficient, ε is the gain compression factor, N_tr is the transparency carrier density, and N_s is a shift to make g equal to the unpumped absorption at $N = 0$. The compression factor accounts for decrease of gain with increasing photon density. The gain is dependent on both carrier and photon density, so the gain variation $\mathrm{d}g$ can be expanded as

$$\mathrm{d}g = a\,\mathrm{d}N - a_p\,\mathrm{d}N_p \tag{2.45}$$

where the gain derivatives are given by

$$a = \frac{\partial g}{\partial N} = \frac{g_0}{(N + N_\mathrm{s})(1 + \varepsilon N_p)} \equiv \frac{a_0}{1 + \varepsilon N_p}, \tag{2.46a}$$

$$a_p = -\frac{\partial g}{\partial N_p} = \frac{\varepsilon}{1 + \varepsilon N_p} g. \tag{2.46b}$$

In Eq. (2.46a), a_0 is the nominal differential gain, the value at zero photon density, which would be the differential gain if no gain compression is considered.

Small-signal analysis

The modulation response can be derived from the rate equations using small-signal frequency analysis. Assuming small sinusoidal current modulation in the form

$$I(\omega) = I_0 + I_1 \mathrm{e}^{\mathrm{j}\omega t}, \tag{2.47}$$

where I_1 is the modulation amplitude superimposed on the steady-state bias current I_0 and ω is modulation angular frequency, then the small-signal responses for the current and photon densities can be written in similar form:

$$N(\omega) = N_0 + N_1 \mathrm{e}^{\mathrm{j}\omega t}, \tag{2.48a}$$

$$N_p(\omega) = N_{p,0} + N_{p,1} \mathrm{e}^{\mathrm{j}\omega t}, \tag{2.48b}$$

where N_0 and $N_{p,0}$ are the steady-state carrier and photon densities, and N_1 and $N_{p,1}$ are the corresponding small-signal modulation amplitudes. By inserting Eqs. (2.48) into Eqs. (2.43) and eliminating the steady state and second-harmonic terms, the frequency domain equations for small-signal amplitudes N_1 and $N_{p,1}$ remain. By solving the system for $N_{p,1}/I_1$, and recognizing that optical power P_1 is related to photon density, the modulation transfer function $H_\mathrm{int}(\omega) = P_1/I_1$ can be derived as [123]

$$H_\mathrm{int} = \eta_d \frac{h\nu}{q} \frac{\omega_\mathrm{R}^2}{\omega_\mathrm{R}^2 - \omega^2 + \mathrm{j}\gamma\omega} = \eta_d \frac{h\nu}{q} \frac{f_\mathrm{R}^2}{f_\mathrm{R}^2 - f^2 + \mathrm{j}\frac{\gamma}{2\pi} f}, \tag{2.49}$$

where η_d is differential quantum efficiency, $h\nu$ is the photon energy, q is the elementary charge, $f_\mathrm{R} = \omega_\mathrm{R}/2\pi$ is the relaxation resonance frequency and γ is the intrinsic damping factor. The intrinsic transfer function has form of a second-order low-pass filter with a damped resonance peak. The optical power modulation follows the current modulation up to frequencies near f_R, when the response can be enhanced, depending on damping. Beyond the resonance, the response drops off dramatically. The peak of the resonance occurs at frequencies slightly lower than f_R depending on the damping, or there may not even be a peak in case of exceptionally strong damping. The factor $\eta_d h\nu/q$ represents the steady state slope efficiency of optical power dependence on input current.

The relaxation resonance frequency, above threshold, can be approximated as [123]

$$f_\mathrm{R} = \frac{1}{2\pi}\sqrt{\frac{v_\mathrm{g} a N_p}{\tau_p}} = \frac{1}{2\pi}\sqrt{\frac{v_\mathrm{g}\Gamma a}{q\mathrm{V_a}}\eta_i(I - I_\mathrm{th})}, \tag{2.50}$$

where N_p and I are steady-state values, and I_{th} is the threshold current. As previously pointed out, the relaxation resonance frequency fundamentally determines how fast an intrinsic diode laser can be modulated when the damping is not severe. Pursuit of higher bandwidth in large part means finding a way to increase the relaxation resonance frequency. From Eq. (2.50), most obvious way to increase f_{R} is to increase the photon density, i.e., by increasing current. However, that even faster increases the damping, but also degrades efficiency and increases heat generation. What is more desirable is to improve the intrinsic laser parameters. Increasing the differential gain a, decreasing the photon lifetime τ_p, increasing the confinement factor Γ or equivalently reducing the mode volume $\mathrm{V} = \mathrm{V_a}/\Gamma$, are the ways the laser can be engineered to improve the relaxation resonance frequency. Often, all these lasers parameters are grouped together into a single figure of merit: the D-factor, which is commonly used to evaluate how efficiently an intrinsic laser can be modulated. The D-factor can be defined as

$$D \equiv \frac{f_{\mathrm{R}}}{\sqrt{I - I_{\mathrm{th}}}} = \frac{1}{2\pi}\sqrt{\frac{v_{\mathrm{g}}\Gamma a}{q\mathrm{V_a}}\eta_i}. \tag{2.51}$$

The damping represents the rate of energy loss in the laser cavity, and the damping factor γ is given as [123]

$$\gamma = v_{\mathrm{g}} a N_p \left(1 + \frac{\Gamma a_p}{a}\right) + \frac{1}{\tau_{\mathrm{d}N}} + \frac{\Gamma \beta_{\mathrm{sp}} R_{\mathrm{sp}}}{N_p}, \tag{2.52}$$

where $\tau_{\mathrm{d}N}$ is differential carrier lifetime. The damping factor is proportional to f_{R}^2, and can be rewritten using Eq. (2.50) as

$$\gamma = K f_{\mathrm{R}}^2 + \gamma_0. \tag{2.53}$$

The K-factor is given by

$$K = 4\pi^2 \tau_p \left(1 + \Gamma \frac{a_p}{a}\right) = 4\pi^2 \left(\tau_p + \frac{\varepsilon}{v_{\mathrm{g}} a}\right), \tag{2.54}$$

where Eqs. (2.46) have been used, and the damping factor offset γ_0 is

$$\gamma_0 = \frac{1}{\tau_{\mathrm{d}N}} + \frac{\Gamma \beta_{\mathrm{sp}} R_{\mathrm{sp}}}{N_p}. \tag{2.55}$$

As illustrated on Fig. 2.15a, increasing the bias current increases the resonance frequency but it also increases the damping even faster. Initially the bandwidth will be increasing until damping becomes too large and limits the bandwidth. Therefore, it is desirable to reduce this effect by reducing the K-factor, which implies that the differential gain should be high and photon lifetime reduced, same as for f_{R}. The effect of K-factor on modulation transfer function is illustrated on Fig. 2.15b, for the fixed bias level and D-factor. The damping factor offset γ_0 is important at low currents when the relaxation resonance frequency is small, and is often not considered [95, 171]. In practice, K-factor and γ_0 are used as fitting parameters extracted from experimentally measured laser modulation response.

The modulation bandwidth is commonly determined by the frequency at which the modulation response drops by 3 dB. In case the damping is small and parasitics do not limit the bandwidth, the 3-dB frequency is given by

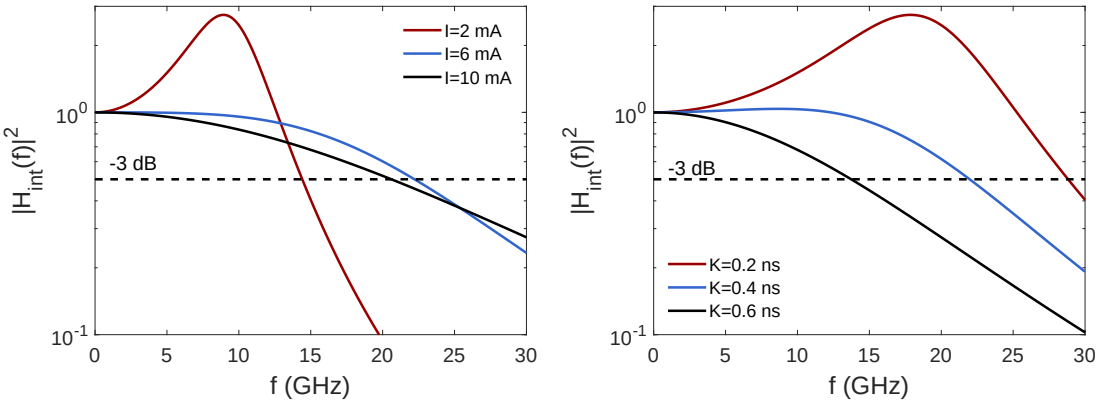
$$f_{3\mathrm{dB}} = \sqrt{1 + \sqrt{2}} f_{\mathrm{R}} \approx 1.55 f_{\mathrm{R}}. \tag{2.56}$$

The theoretically maximum $f_{3\mathrm{dB}}$ limited by damping is when $\gamma/\omega_{\mathrm{R}} = \sqrt{2}$ [123], which gives

$$f_{3\mathrm{dB}}\big|_{\max} = \sqrt{2}\frac{2\pi}{K}. \tag{2.57}$$

Introduced already in previous chapter, a figure of merit used commonly to estimate the overall high-speed performance is MCEF, defined in similar way as D-factor [70]:

$$\mathrm{MCEF} \equiv \frac{f_{3\mathrm{dB}}}{\sqrt{I - I_{\mathrm{th}}}}. \tag{2.58}$$



(a) (b)

Figure 2.15: Examples of simulated intrinsic modulation transfer function for (a) varying pumping current levels assuming $D = 10\,\mathrm{GHz/mA^{0.5}}$, $K = 0.4\,\mathrm{ns}$, $I_{\mathrm{th}} = 1\,\mathrm{mA}$ and (b) varying K-factors assuming fixed $D = 10\,\mathrm{GHz/mA^{0.5}}$, $I = 5\,\mathrm{mA}$, $I_{\mathrm{th}} = 1\,\mathrm{mA}$.

The Fig. 2.16 illustrates how $f_{3\mathrm{dB}}$ depends on pumping and damping levels. In case of negligible damping, the $f_{3\mathrm{dB}}$ follows the square root of bias current, same as resonance frequency. With damping, the $f_{3\mathrm{dB}}$ deviates from this trend and with increasing bias saturates at level given by Eq. (2.57). With further increase it becomes lower. The stronger the damping is, the larger is deviation and quicker it reaches the maximum level. It can be concluded that the K-factor is the parameter that defines the intrinsic modulation bandwidth capabilities of the laser.

The gain compression ε affects both D-factor and K-factor. In D-factor, ε figures through the differential gain a and its influence depends on photon density, so it negatively influences the resonance frequency at higher injection levels. In K-factor, it shows also independent of the photon density, and its increase enhances the K-factor.

In given analysis any transport time for carriers to reach the active region has been neglected. However, these carrier transport effects can influence the bandwidth significantly for lasers with

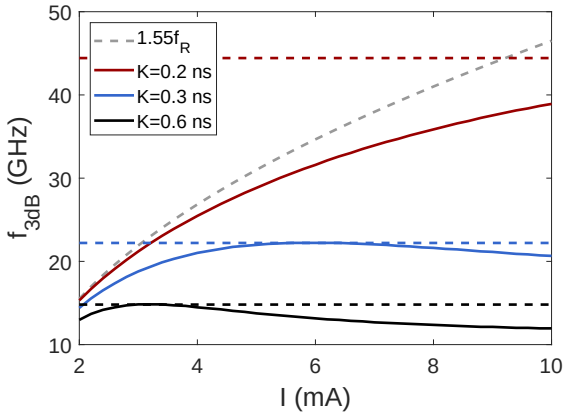


Figure 2.16: 3-dB frequency as a function of bias current for varying K-factors assuming fixed $D = 10\,\mathrm{GHz/mA^{0.5}}$ and $I_{\mathrm{th}} = 1\,\mathrm{mA}$. The gray dashed line represents the 3-dB frequency in case of no damping as estimated by Eq. (2.56). The horizontal dashed lines represents maximum 3-dB frequency limited by damping as given by Eq. (2.57).

quantum-well active regions with separate-confinement heterostructures (SCHs). These effects can be considered by replacing the carrier density rate equation with two separate equations for carrier densities in barrier and active regions. The small-signal analysis results in similar set of equations with two modifications. A new term χ called the transport factor appears, which effectively reduces the differential gain to a/χ and increases the differential carrier lifetime to $\tau_{\mathrm{d}N}\chi$. This reduces the resonance frequency and increases the K-factor. The second modification is that a new prefactor appears in modulation transfer function which acts as low-pass filter and reduces the bandwidth in similar way as extrinsic parasitic response [123].

Another effect that was not considered is the temperature dependency of laser parameters. High temperature degrades the differential gain, reduces the injection efficiency, increases the threshold current and redshifts the cavity mode and gain peak. All these generally lead to a reduction of the bandwidth, therefore heat management becomes increasingly important for high-speed lasers.

Pushing the limits of speed is more challenging for long wavelength VCSELs due to material properties. Auger recombination is more present which enhances the thermal effects. The differential gain is usually inherently lower. In previous section, the challenge of mirrors has been discussed, which influence the photon life time or effective cavity volume. All this has contributed to slower development of high-speed LW-VCSELs, compared to VCSELs for shorter wavelengths.

2.4.2 Controlling the photon lifetime

From the previous analysis it can be concluded that intrinsic modulation bandwidth is determined by relaxation resonance frequency and damping, i.e., D-factor and K-factor. Improvement of the bandwidth can be achieved by increasing the D-factor and reducing the K-factor. From derived expressions, it can be seen that both these effects can be achieved in a same way: by increasing the differential gain and reducing the photon lifetime.

Differential gain can generally be enhanced by introducing strain and increasing the number of QWs [123]. In this work, the differential gain enhancement has not been investigated, and the focus has been on reducing the photon lifetime.

The photon lifetime is determined by the internal and mirror losses. As the threshold gain was defined in similar way, we can write

$$\frac{1}{v_{\mathrm{g}}\tau_p} = \Gamma g_{\mathrm{th}}. \tag{2.59}$$

Starting from the amplitude condition, given by Eq. (2.25), the expression for photon lifetime can be written as

$$\frac{1}{\tau_p} = v_{\mathrm{g}}\left(\langle\alpha_i\rangle + \frac{1}{2\mathrm{L}_{\mathrm{eff}}}\ln\left(\frac{1}{R_{\mathrm{t}}R_{\mathrm{b}}}\right)\right), \tag{2.60}$$

where $\langle\alpha_i\rangle$ is average internal loss from all parts of the cavity, $\mathrm{L}_{\mathrm{eff}}$ is the effective cavity length, and $R_{\mathrm{t,b}} = |r_{\mathrm{t,b}}|^2$ are the top and bottom mirror reflectivities. From Eq. (2.60), three ways to reduce photon lifetime can be identified: increasing the internal losses, reducing the effective cavity length and reducing the mirror reflectivities. Increasing the internal losses is a bad idea as it leads to pure non-radiative losses and reduction of differential quantum efficiency.

Modifying the reflectivity has been successfully used to tune the photon lifetime. Lowering the reflectivity of one or both mirrors reduces the photon lifetime without degrading the differential quantum efficiency, but it also increases the threshold gain and therefore threshold current, so there is a trade-off. Simplest way to achieve this is to reduce the number of pairs of DBR, however this may lead to increase of device resistance in case of epitaxial mirrors on which contacts are formed. More precise photon lifetime tuning can be done, for example, by shallow surface etching [72, 172] or by depositing $\mathrm{Si}_x\mathrm{N}_y$ [85].

Reduction of the cavity length has similar effect. It is important to notice that here the effective cavity length is considered. Equivalently, it can be considered as reduction of mode volume or increase of confinement factor. This can be achieved in two ways: by reducing the length of the cavity itself and by minimizing the penetration depth of the mirrors. VCSELs with cavities as short as 0.5-λ [74, 84] have been demonstrated, with significant improvement of the modulation

bandwidth. On the other hand, use of dielectric DBRs, with significantly shorter penetration depth, has also been shown to contribute to speed enhancement [94].

HCGs offer a possibility to reduce the photon lifetime without decreasing the reflectivity [106]. As discussed before, the penetration depth of HCGs can be much shorter than even dielectric DBRs, and it can be controlled by engineering the grating parameters.

2.4.3 Transverse mode confinement

For high-speed VCSELs, increasing photon density is beneficial. By ensuring the single-mode operation, photons do not spread among the other modes, and photon density increase with current increase is maximized. The longitudinal modes are defined by free spectral range of the cavity, which is reversely proportional to cavity length. For VCSELs, due to short cavity length, free spectral range is relatively large and the single longitudinal mode is guaranteed due to spectral dependence of gain. The transverse mode spectral separation is much smaller and multiple modes could be supported by the gain spectrum. Therefore, the laser design should be engineered to give highest overlap for only fundamental mode and suppress any higher transverse modes.

Confinement factor is one of the key parameters of the lasers. It determines the portion of the field that experiences gain and therefore has significant influence on the performance of the lasers, such as threshold current, modulation speed, single-mode property, and output beam profile. Total confinement factor Γ was introduced in Eq. (2.39). It was then split into longitudinal and transverse component. The longitudinal confinement factor is generally small for VCSELs ($< 10\%$) due gain being present only in thin layer along the light path within the resonator, so the transverse confinement needs to be as high as possible to reach sufficient total confinement for low threshold lasing. The longitudinal confinement factor and the ways to increase it were already discussed in previous sections, and here the transverse confinement is considered.

The transverse confinement factor describes the overlap of the lasing mode's transverse field profile with active region. Therefore, it depends on both the mode profile and the geometrical shape of active region, i.e., current confinement. While they can be controlled independently, often methods for controlling the optical mode also influence the current confinement, and vice versa. In this section focus will be on optical confinement, while current confinement will be discussed more in next chapter.

Optical confinement can be achieved by forming a waveguide in longitudinal direction. If one of the cavity parameters in transverse direction is varied, it would lead to different resonance wavelength in different cavity regions. By considering the effective refractive index, it can be shown that local shift of the resonance wavelength $\Delta\lambda$ results in corresponding change of the effective refractive index Δn_{eff} in that region [173]:

$$\frac{\Delta n_{\text{eff}}}{n_{\text{eff}}} \approx \frac{\Delta\lambda}{\lambda}. \tag{2.61}$$

By designing a core and a cladding region with lower effective refractive index, a waveguide (or lens-like structure) can be formed and field will be more confined to the core of the waveguide, favoring the fundamental mode. Different transverse modes would extend to various degree into the cladding region, so the higher-order modes, which extend more into the region of lower effective index and therefore have a lower effective mode index, will have shorter resonance wavelengths [174]. With sufficient wavelength change, higher transverse modes may not be supported and their lasing will be suppressed. The resonance wavelength can be shifted in several ways, like modifying mirror reflectivities and reflection phases, or by modifying cavity optical length through refractive-index change. Confinement can also be achieved through gain guiding and thermal lensing. Gain guiding appears when the current is confined to a small aperture [175]. Then, the high concentration of carriers in that region changes the imaginary part of the refractive index and causes confinement of light towards the gain region. However, carriers also reduce the real part of refractive index, which causes antiguiding, so gain guiding is often not strong enough to ensure single-mode operation by itself. Furthermore, high intensity field of the fundamental mode results in depletion of the carrier density, an effect known as spatial hole burning, which disrupts the guiding property [174]. The

thermal lensing comes from the temperature dependence of refractive index and the temperature distribution that results from self-heating due to resistive loss. Even in structures where gain and thermal guiding are not the primary methods of optical confinement, they are always, more or less, present and contribute to final modal property of the laser.

Various confinement methods are illustrated on Fig. 2.17. Some of the simplest ways to provide optical confinement are [65]: (a) finite lateral size of the mirrors, but the diffraction losses limit the minimum size so the single-mode operation is unlikely; (b) pure gain guiding, which may be unstable at higher injection levels due to spatial hole burning; (c) air-post structure created by mesa etching of the structure, which may cause large non-radiative losses and light scattering at the walls deteriorating the performance.

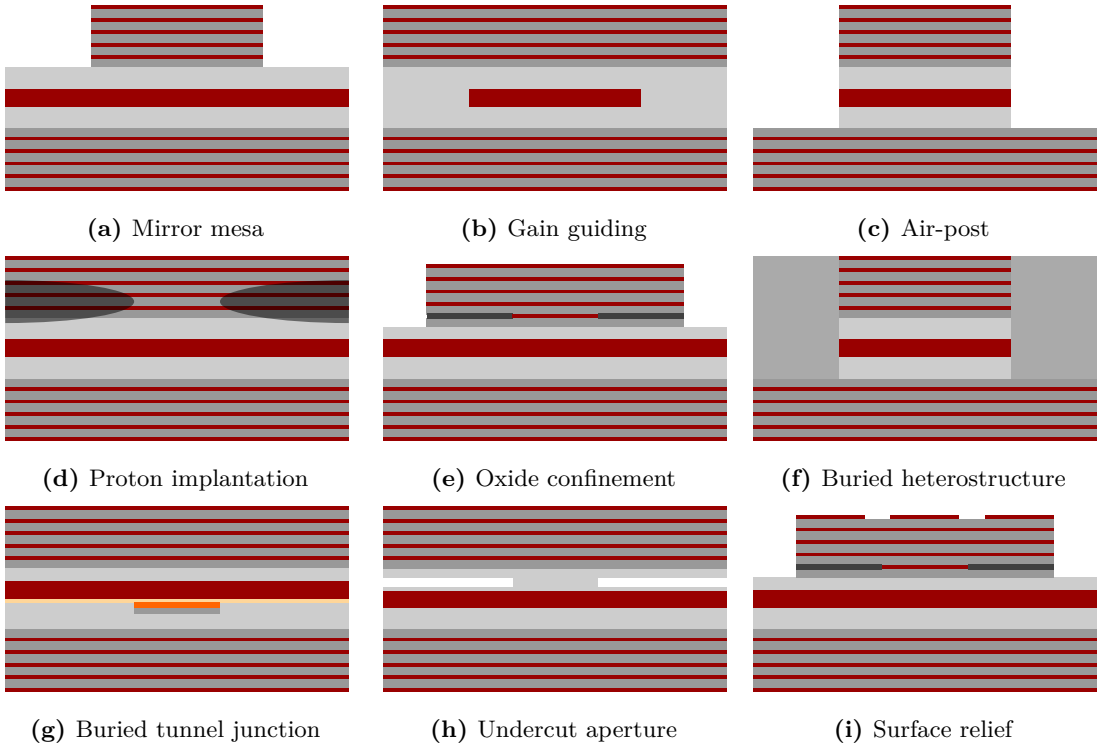


Figure 2.17: Schematic illustrations of different optical confinement methods.

Proton implantation is one of the methods that can be used to create current confinement, and in such way cause gain guiding and thermal lensing. There is a limit to how small apertures can be created and due to unstable nature of guiding mechanisms, proton-implanted VCSELs often are unable to maintain good mode characteristics with higher currents [174].

Very successful method for both current and optical confinement are oxide apertures, created by partial oxidation of a high Al-content layer in one of the AlGaAs-based DBRs, close to the active region. The resulting dielectric prevents current flow outside the aperture and refractive index change from ∼3 to ∼1.6 provides excellent index guiding with good overlap between mode and gain region. Small apertures, needed to ensure stable single-mode operation, can lead to high series resistance and are difficult for fabrication. Such issues can be corrected with more advanced variations, such as tapered [176] or multiple oxide aperture [75, 84], which have been used in record-setting short wavelength VCSELs.

For InP-based VCSELs selective undercut etching of a thin layer, close to the active region, can be done to form an air-gap aperture for transverse current and optical confinement that would be in many ways similar to oxide apertures [177]. With scattering loss being stronger for higher modes, single-mode emission is favored more strongly even with apertures that would large enough

to support higher-order modes in cases of other methods. The drawback is difficult control of exact aperture size and mechanical stability of such free standing structure.

Buried heterostructures can be realized by epitaxial regrowth of the air-post structure [65]. Regrowth material can be semi-insulating or reversely biased so that current confinement is provided, and the refractive index can be lower than the cavity so that index-guiding ensures optical confinement. Challenging fabrication and poor quality of regrown interface are the limits of this design. Buried tunnel junction (BTJ) is more advanced variation of this method. It is formed by patterning only TJ layers immediately after their growth, so that TJ remains only in the center of the device. Then, rest of the epitaxy is grown. Current flow is possible only in the remaining BTJ that forms the aperture, and the change of the effective refractive index provides index guiding. BTJ structures can be very small and single mode emission of the fundamental mode can be achieved. This method has been successfully employed in long wavelength VCSELs leading to excellent performance [95].

Often, one of the described methods is unable to ensure single-mode operation on its own at larger powers or if the aperture is too large. In those cases, single-mode operation can be forced by using additional mode-selection mechanism [174]. For example, employing implantation in oxide confined VCSEL or introducing metal aperture on the output side to act as a spatial filter. Losses can be introduced in the perimeter of the top mirror that would affect higher modes more than the fundamental mode. Patterning the photonic crystal structure in the top mirror [178] and various surface reliefs patterned in the surface of the top mirror [179, 180] can be used to discriminate higher modes. Finally, the HCG heterostructures introduced previously can also provide transverse mode selection [141, 143].

2.4.4 Chosen design

In this work, hybrid long wavelength VCSELs are investigated with main interest in achieving high modulation bandwidth. The intrinsic response is improved by the reduction of the effective cavity length and mode volume, mainly by employing mirrors with extremely short penetration depth.

From the discussion given in this chapter, it can be concluded that the HCG reflector and dielectric DBR have advantage over epitaxial DBRs. With much shorter penetration depths, use of this mirror types can significantly reduce the effective cavity length. HCGs optimized for TM polarization show large improvement over TE-optimized HCG in terms of evanescent field penetration, which enables further reduction of total cavity length.

Hybrid design in this work makes it possible to implement bottom HCG reflector. The grating is etched in the Si layer of the SOI wafer. Since Si has larger refractive index than III-V materials, such Si/air grating has larger refractive-index contrast than III-V/air gratings, which results in broader reflection bandwidth. Below the grating is low-refractive-index BOX layer. Above the grating, low refractive index can be realized as an air gap by sacrificial etching or as deposited dielectric layer.

Top mirror can be another HCG, realized as a III-V/air membrane. However, due to easier fabrication, dielectric DBR is implemented as a top mirror, using a-Si and SiO_2 as high and low refractive index materials. Due to high refractive-index contrast, only 3–6 pairs can be sufficient for high reflection.

Hybrid VCL based on this design has been previously demonstrated with optical pumping. With design that uses thin air gap above the TM HCG and SiO2/a-Si ($\Delta n = 1.47$) DBR with 6 pairs, demonstrated 3-dB frequency was above 27 GHz, limited by the pumping setup, with MCEF=42.1 GHz/mA$^{1/2}$ [120]. Further numerical analysis showed that intrinsic response of the laser could potentially be even faster with bandwidth >40 GHz [121].

The schematic illustration of the hybrid VCSEL structure investigated in this work is shown on Fig. 2.18. Bottom mirror is 480 nm air/Si HCG reflector with reflectivity higher than 99.9%, optimized for TM polarization, with 1 μm SiO_2 layer below the grating and <200 nm SiO_2 layer above the grating. Silica is chosen instead of air due to easier fabrication and better reliability and stability, even though layer thickness is slightly higher compared to equivalent design with air gap. Top mirror is SiO_2/a-Si DBR, with only 3 pairs reaching reflectivity higher than 99.6% due to

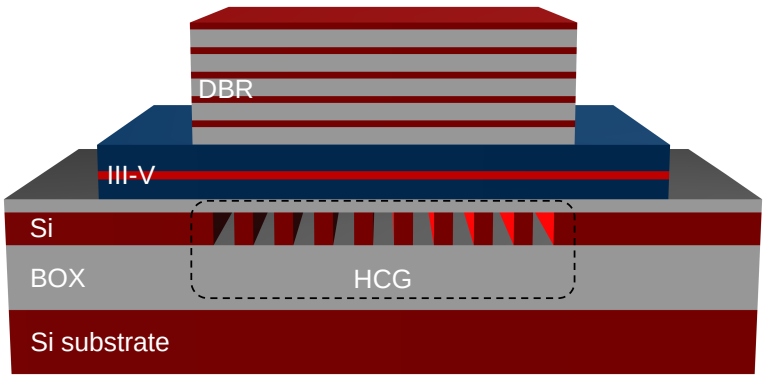


Figure 2.18: Schematic illustration of the hybrid VCSEL structure investigated in this work. The cavity is formed between dielectric SiO_2/a-Si DBR and air/Si TM HCG. The III-V epitaxy contains active region shown in bright red.

improved $\Delta n = 2.22$. The transverse confinement is ensured by implementing the heterostructure HCG. The grating paramters are varied gradually in steps every Λ distance in both directions. At every step additional offset is added. This gives compromise between abrupt and adiabatic change.

More detailed design will be given later in chapter 4 for each fabricated design depending on the epitaxy structure that was used.

2.5 Summary

In this chapter optical design of the VCSELs is discussed with focus on different mirror technologies and high intrinsic modulation speed.

HCGs are introduced as an attractive alternative for VCSEL mirrors. The physics of the HCG reflector is shortly described and some of the key features are discussed. The polarization selectivity is explored and it was shown that TM optimized HCGs have much shorter evanescent field penetration depth compared to TE HCGs. This feature is exploited in the design of the lasers investigated in this work.

One of the biggest obstacles in development of long wavelength VCSELs has been the technology of the mirrors that form the cavity. In this chapter, some of the most successful mirror designs are reviewed and compared. Key properties of the mirror design and how they influence the laser performance are discussed.

Basic theory of intrinsic modulation response of the lasers is given, which provided insight into best ways to increase the modulation bandwidth. The photon lifetime has been identified to be the key property as both the resonance frequency and damping can be both improved by reducing photon lifetime. The best way to achieve that is to reduce the effective cavity length.

The optical design of the VCSELs investigated in this work is given. The hybrid III-V-on-Si design employs HCG as a bottom mirror and a dielectric DBR with high refractive-index contrast as a top mirror. Extremely short penetration depth of the field into these mirrors leads to reduction of the effective cavity length and improvement of the modulation bandwidth.

CHAPTER 3

Electrical pumping of VCSELs

3.1 Introduction

Electrical injection of carriers is critical property for many applications of lasers and electrically pumped semiconductor lasers are the most widely used type of lasers. In application for optical communications, it makes it possible to transfer information from electrical to optical domain directly by modulating current that pumps the laser. Optical pumping of semiconductor lasers is also possible, but it requires another laser source, which decreases the efficiency and increases the complexity and price of such systems. It is only used in case when electrical injection is not possible. While electrical pumping makes lasers easier to use, the device structure itself is more complex. Additional to the optical phenomena discussed in the previous chapter, the electrical phenomena need to be also considered when designing semiconductor lasers.

Electrically, a laser is a PIN diode, with active region comprising the intrinsic (i) part of the diode which is pumped with carriers under forward bias. Passive regions of the diode need to be p- and n-doped so that they become conductive with low resistance and ohmic contacts need to be formed between doped semiconductor and metal contact pads. Current needs to be directed to pump the region where the optical mode would be the strongest. Mesa size needs to be small to reduce the capacitance of the device. All the various resistive and capacitive phenomena on the current's path through the laser together determine both the static current-voltage (I–V) characteristic and the small signal parasitic response $H_{\mathrm{par}}(f)$. Lowering differential resistance reduces the overall power consumption of the laser and gives steeper slope of I–V characteristic, which means that smaller voltage swing can be used to sufficiently modulate the current, so driving electronics can be more efficient also.

Design of the VCSEL presented in this work has been previously investigated under optical pulsed pumping [64, 120]. In those works, pumped region is defined by the beam spot of the pump laser, and there is no lateral carrier confinement structure. There is no need for doped layers or contacts. The small signal modulation is provided by modulating the pump laser beam using external modulator. In this work, electrical pumping is implemented with goal to preserve the excellent intrinsic performance of the design. In this chapter, the parasitic electrical elements and how they influence the performance of lasers are discussed. Methods for current confinement, using proton implantation and undercut etching, are investigated and ohmic contacts to InP are tested for lowest contact resistance and good reliability.

3.2 Electrical pumping for high-speed

Direct high-speed modulation of the diode laser depends not only on the dynamics of the interaction between the carriers and photons, but also on the electrical behavior of the whole device. From contact pads to confined current flow in active region, all electrical phenomena combined determines the high-speed performance of the laser diode.

3.2.1 Extrinsic parasitic response

In previous chapter, the total modulation frequency response was given as product of intrinsic and parasitic contributions (see Eq. (2.42)). The intrinsic response has been shown to have form of a second-order low pass filter as given by Eq. (2.49).

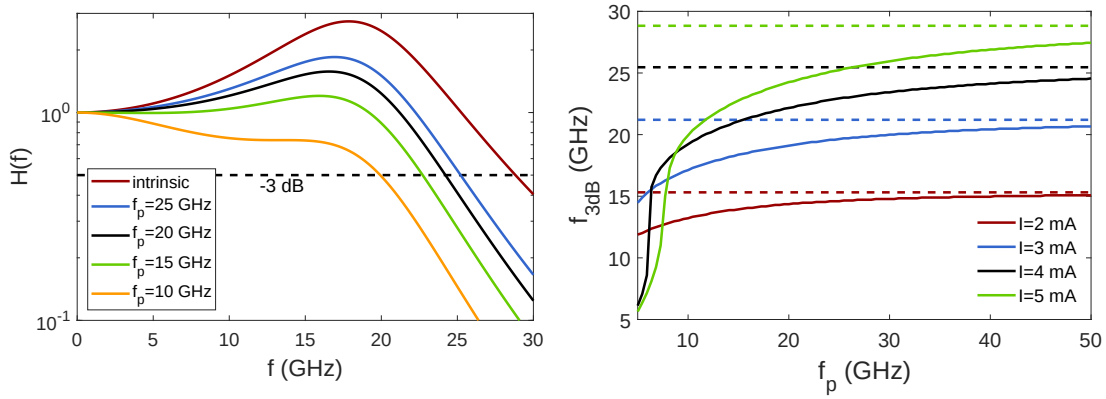
The parasitic response is obtained as a ratio between the current flowing into the intrinsic diode and applied voltage. It can be described approximately by a single-pole low-pass filter function [181]:

$$H_{\mathrm{par}}(f) = \mathrm{const} \times \frac{1}{1 + \mathrm{j}\frac{f}{f_{\mathrm{p}}}}, \tag{3.1}$$

where f_{p} is parasitic cut-off frequency determined by the RC time constant (any inductance is usually so small that it can be neglected) of the device. By substituting Eq. (2.49) and Eq. (3.1) into Eq. (2.42), the overall modulation transfer function can be written as:

$$H(f) \sim \frac{f_{\mathrm{R}}^4}{(f_{\mathrm{R}}^2 - f^2)^2 + \left(\frac{\gamma}{2\pi}\right)^2 f^2} \cdot \frac{1}{1 + \left(\frac{f}{f_{\mathrm{p}}}\right)^2}. \tag{3.2}$$

The additional low-pass filter effect of parasitic response will lower the overall response compared to intrinsic response, as is illustrated on Fig. 3.1a, which shows the overall transfer function for different parasitic cut-off frequencies and fixed intrinsic transfer function given by red line. The Fig. 3.1b shows how the 3-dB frequency is influenced by the parasitic response at different bias levels. At low current, when intrinsic bandwidth is lower than f_{p}, the bandwidth reduction is small. As the intrinsic bandwidth rises with increasing current above the f_{p}, the overall bandwidth is more and more strongly affected by parasitics. In order for the bandwidth to reach the intrinsic potential, the parasitic cut-off frequency needs to be significantly higher.



(a) **(b)**

Figure 3.1: (a) Examples of simulated overall modulation transfer function for varying parasitic cut-off frequencies assuming $D = 10\,\mathrm{GHz/mA^{0.5}}$, $K = 0.2\,\mathrm{ns}$, $I_{\mathrm{th}} = 1\,\mathrm{mA}$ and $I = 5\,\mathrm{mA}$. (b) 3-dB frequency as a function of parasitic cut-off frequency for varying bias current. The horizontal dashed lines represent the 3-dB frequency of only intrinsic response.

3.2.2 Parasitic elements

Parasitic response is often one of the main limiting factors for high-speed lasers and increasing the parasitic cut-off frequency is of critical importance for pushing the modulation bandwidth. For that purpose, all parasitic resistive and capacitive elements of the device need to be minimized.

The parasitics depend on device structure, design geometry and material properties. Therefore, every VCSEL design has different parasitic elements. In general case, parasitics can be split into two groups: parasitics of contact pads and parasitics from diode chip. In simplest small-signal circuit model, each can be modeled with single resistor and capacitor, and these two parasitic groups are connected in parallel as shown in Fig. 3.2 [182]. On one side this circuit is connected to the high frequency driving signal generator and on the other side to the active region with the junction resistance R_j. The goal is to maximize the current that goes into the active region branch by minimizing the series resistances and increasing the impedance of the parallel branches with capacitances.

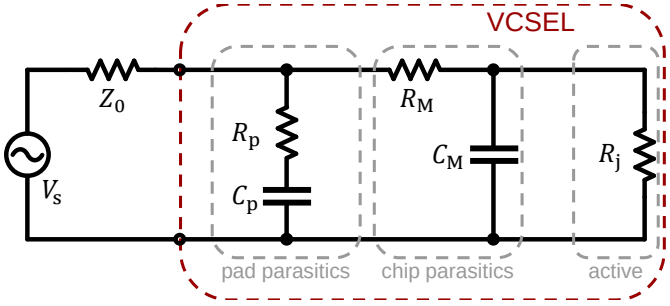


Figure 3.2: Small-signal simplified circuit model of a VCSEL connected to high frequency driving signal generator V_s with impedance Z_0. The VCSEL is comprised of pad parasitics, chip parasitics and diode junction resistance, connected in parallel [182].

Pad parasitics

The R_p accounts for the resistive loss in the pads. Usually, pads are formed with thick gold layers so the resistance is relatively small and can be neglected from small-signal models.

The C_p represents the pad capacitance between the signal and ground metal contacts. It strongly depends on the pad layout and the materials between the pads. Their surface size should be minimized, but it is limited by the size of the probes or bonded wires. It can be minimized by reducing the overlap of the pads and by using thick layer of dielectric with low permittivity between them, such as benzocyclobutene (BCB) [183, 184], polyimide or silicon dioxide. Undoped or semi-insulating substrates also help reduce the pad capacitance.

The pads of the VCSELs in this work are realized with thick layer of gold. There is no overlap between the pads and they are made to be coplanar, by depositing them on a layer of BCB. Since the substrate is SOI, the capacitance towards the substrate is also minimal.

Chip parasitics

There are several sources of resistance on the current path through the laser diode, as illustrated on the VCSEL example shown in Fig. 3.3. The intrinsic diode junction inside the aperture is represented by R_j. This is where stimulated recombination is happening and where most of the current should go. It depends on the diode junction properties, but also on the geometry of the aperture. The blocking layers that form the aperture are assumed to be perfect, i.e., resistance is very high and can be neglected from the model. R_{top} and R_{bot} represent series resistance on the current path from ohmic contacts to aperture and intrinsic region. Contact resistance of ohmic contacts is the first contribution to series resistance, although it is usually small, in ohm range. Next series resistance on the current path is the general sheet resistance of the contact layers, which depends on the doping. In this example, top contact is shown to be made on top of DBR, so main contribution to R_{top} is the resistance of the doped epitaxial DBR. In general, alternating layers will have higher series resistance compared with bulk doped semiconductor layer. Bandgap-engineering

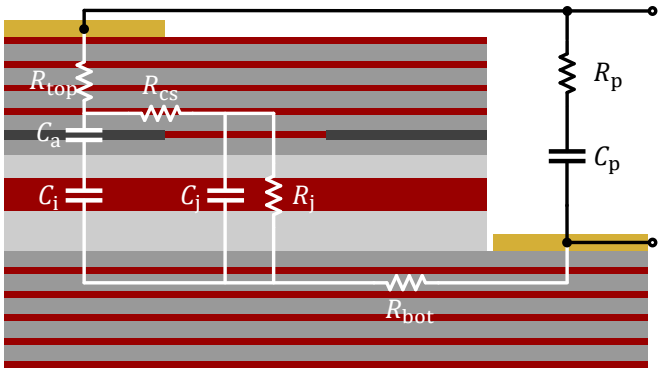


Figure 3.3: Electrical parasitic elements superimposed on cross-sectional schematic of a VCSEL with double DBR structure with one intra-cavity contact, as an example.

schemes can be used to reduce these losses. Intra-cavity contacts, as illustrated for bottom contact in this example, can be used to avoid current going through the DBR. This is mandatory for lasers that employ dielectric DBRs. The issue with intra-cavity contacts is uniformity of current spreading due to shorter thickness and higher optical losses due to higher doping need for contact layers [185]. Short-cavity lasers, with intra-cavity contacts and thin contact layers, in particular can suffer from poorer current spreading. Due to existence of aperture, the current is forced to spread laterally. This is modeled by R_{cs} which accounts for lateral spreading resistance and the voltage drop at the heterobarriers around the active region. Current spreading is desirable to facilitate injection of carrier into center of the aperture and avoid current crowding at the aperture edges. This can be achieved by increasing the doping concentration [186]. Alternatively, by inserting additional resistive layer between contact layers and active region will enhance lateral spreading of current at the price of slight increase in series resistance.

The chip capacitance is comprised of three contributions marked with C_j, C_a and C_i on Fig. 3.3. C_j represents the diode junction capacitance inside the aperture, where current flows. It is connected in parallel with R_j and, under normal forward bias condition, it is dominated by the diffusion capacitance of minority carriers in the intrinsic region [187]. The C_i is the capacitance of the same layer, but in the region where the current is not flowing, underneath the aperture layer. It is connected in series with C_a, which is the capacitance of the non-conductive part that forms the aperture. For oxide-confined VCSELs, this is simply the oxidized layer and, since they are usually thin, their capacitance can be significant. To reduce it, additional non-conductive layers can be added, which would have low capacitance that would be connected in series with C_a, e.g. double or multiple oxide aperture layers [73, 188] or thick proton implanted regions [189]. In case of the buried tunnel junction apertures, the C_a is capacitance of depletion region of reverse-biased *pn*-junction outside of aperture [95]. C_a and C_i can both be reduced by reducing the mesa size.

3.2.3 Tunnel junction

Compared to electrons, the holes have significantly lower mobility ($\mu_e/\mu_h \approx 20$), which gives higher resistances in *p*-type doped semiconductor layers compared to *n*-type materials. *p*-type materials also exhibit higher free carrier absorption, which causes higher optical losses, and ohmic contacts to *p*-type contact layers show higher contact resistances. In a laser diode device, the high series and spreading resistances, which can be dominated by the *p*-doped layers, lead to increase in self-heating and lower parasitic response. Therefore, it is desirable to avoid *p*-type conductive layers.

This can be achieved by including the tunnel junction (TJ) structure on *p*-side of the diode [89, 190, 191]. The TJ consists of heavily *p*- and *n*-doped low-bandgap layers. Due to heavy doping,

under reversed bias conduction band electron states on the n-side become aligned with valence band hole states on the p-side. The electrons can then easily tunnel through, and such p^+n^+-junction shows an ohmic behavior with very low resistance. By incorporating the TJ on p-side of the laser diode, the hole current can be converted to electron current so the major part of contact layer on p-side of the laser diode can also be n-type.

Compounds with small bandgap can be used for LW-VCSEL InP-based devices, which is advantageous for extremely small tunnel junction resistances [90]. The use of TJ leads to lower electrical resistance and reduced heat generation, which is of critical importance for LW-VCSELs. Low-resistive n-type ohmic contacts can be used on both sides and lower spreading resistance enables the use of intra-cavity contacting scheme [191]. Optical losses are reduced by use of n-type, but the TJ needs to be placed at the minimum of the optical field intensity within the VCSEL cavity in order to avoid significant free-carrier absorption in highly doped layers [192].

The TJ can be patterned to create buried heterostructures that provide efficient optical and current confinement. These structures will be discussed more in next section.

3.3 Current confinement

As already discussed in section 2.4.3, current confinement is of paramount importance for achieving high confinement factors and excellent performance. The transverse confinement factor of VCSELs needs to be high, so overlap of current injection and optical mode needs to be maximized. In section 2.4.3, the optical confinement methods were reviewed, but in most cases they also provide current guiding and confinement. In this section some most common current confinement methods are reviewed. Apart from guiding current, confinement methods can significantly affect parasitics of the laser, so their design should be optimized for high-speed operation.

3.3.1 Current confinement methods

Some of the current confinement methods are already illustrated on Fig. 2.17.

The ring shaped electrode can be used to guide the current, with light emission from central opening. However, without any additional confinement method, the current will spread due to diffusion. Air-post structure can be used to limit the current in small volume and is simple to fabricate, although non-radiative recombination on exposed surface may be significant. This can be avoided with buried heterostructure, but the fabrication of such devices is more complex [65].

Ion implantation is another method for current guiding that is easy to implement. Most commonly used ion is proton. Damages created in doped semiconductors increase their resistivity and, with sufficient dose, can render them non-conductive. It is a common method often used in conjunction with other methods, to ensure additional current and optical guiding [174] and to reduce the capacitance [189].

For GaAs-based SW-VCSELs, most successful current confinement method are oxide apertures, formed by partially oxidizing thin Al-rich AlGaAs layers. While the oxide blocks the current flow outside the aperture opening and provides good optical confinement, the downside of this method is relatively large capacitance C_a of such thin layers. The capacitance can be reduced by using additional proton implantation, as mentioned above, or by forming multiple oxide apertures, their capacitances would be connected in series and total capacitance would be reduced, at the cost of slight increase in resistance [171, 188]. Such multiple oxide apertures have been used in SW-VCSELs with highest demonstrated bandwidth to date [75, 84].

Tunnel junction can be laterally patterned to create buried heterostructure [193]. This can be achieved using two epitaxial growth runs. In first growth run, the VCSEL structure is grown, stopping after TJ layers on p-side of the diode. Then the n^+- layer is etched outside the aperture area. The second epitaxial growth is then done, where n-type current spreading and contact layers are regrowth, starting with low doping concentrations. In etched region, the resulting p^+n-junction is blocking under reverse bias, allowing the current to flow only in the unetched aperture area with the ohmic p^+n^+-junction [91]. Such buried tunnel junction (BTJ) aperture can have very

small dimensions and provide also optical guiding. BTJ have been employed in some of the best performing LW-VCSELs [95].

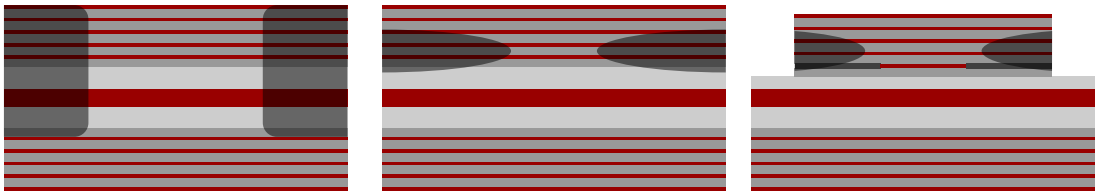
An alternative approach used for LW-VCSELs are undercut apertures created by selective partial lateral etching of a thin layer, leaving an air-gap that would provide perfect current blocking and index guiding. The layer that is etched can be the active region itself, a separate layer near the active region or the TJ layers [194]. Similar to the oxide apertures, capacitance of such apertures can be issue, but also the exposed sides may cause surface recombination.

Current confinement was one of the biggest challenges for the laser design proposed in this work. Two most successful methods, oxide aperture and BTJ, were not available. Selective oxidation is not possible since the materials are InP-based and the regrowth process needed for implementing BTJ is very difficult to implement with hybrid wafer bonded structure. Therefore, alternative methods for current confinement were investigated. The device mesa size is reduced so that current is confined in as small volume as possible similar to the air-post structure. Proton implantation and selective undercut etching were explored as methods for creating apertures.

3.3.2 Ion implantation for current confinement

VCSELs with ion implantation

In VCSEL technology, implant isolation has been used for several purposes, illustrated on Fig. 3.4. The multi-energy broad implantation can be done to electrically isolate the devices [195]. It is an alternative to mesa etching to avoid non-radiative surface recombination and maintain planar surface. Narrower implantation can be used as primary method for creating aperture [196], or for additional mode-selection by shaping gain guiding in oxide aperture. It is also used for reducing the capacitance of oxide apertured VCSELs by increasing the overall thickness of the blocking region [189].



(a) Device isolation **(b)** Implanted aperture **(c)** Combined with oxide aperture

Figure 3.4: Schematic illustrations of ion implantation use in VCSELs.

Compared with BTJ, the ion implantation is significantly simpler to fabricate as it is planar process and doesn't require additional epitaxial growth. Compared to undercut etching, it offers simpler control and greater flexibility of aperture size and shape.

Ion implantation as a method of creating apertures has its disadvantages. The spreading of ions and crated vacancies in both longitudinal and lateral direction is unavoidable and has to be taken into account when designing the aperture shape and when ion energies are chosen. This puts limit to minimum size of the aperture. The dose also needs to be chosen carefully. Too low dose will result in lower resistance of implanted layers, leading to current leakage, while too high dose can result in excess damage of the contact layers above the targeted area, which can lead to high contact resistance.

Apertures formed by ion implantation are most commonly positioned within the *p*-type DBR, close to the active region but without damage spreading to the active region itself. If the implantation is done from the *n*-side, through the cavity layers, the implantation dose and energy need to be carefully optimized to minimize the damages in active region and usually the devices need to be annealed at temperatures up to 400 °C for short time to recover the damage [196]. In case of devices which employ the TJ, the aperture can be created by implanting the TJ layers to block the tunneling [112, 197].

Considering that no epitaxial DBRs are used in proposed laser design, the implantation of TJ was chosen. However, due to epitaxy design, the TJ is positioned below the QW region after the epitaxy is flipped for bonding. So, the implantation has to be done through the active region. Furthermore, the cladding between the QWs and the TJ is very thin, about 30 nm, meaning that it is impossible to avoid damage distribution from overlapping with QWs, which would lead to non-radiative recombination at the aperture edges. It is expected that these unwanted damages outside TJ would be recovered during post-implant anneal.

Implant isolation

Ion implantation is used for two purposes: selective doping and implant isolation. The isolation is achieved through introduction of deep-level traps in the band gap, which lowers the conductivity. Two methods can create such deep-levels [198]: chemically active states and damage-related states. The first method relies on implantation of specific ion species that have electronic level in the middle of the bandgap and annealing is usually required to activate the ions, similar to dopants. The second method relies on physical damage of the crystal lattice caused by bombardment with neutral species. Defects, like vacancies, displaced atoms and dislocations, create deep-level trap centers which reduce the concentration of the free carriers and reduce the carrier mobility in the semiconductor.

Thermal stability of implant isolation is of great importance. The damage-related levels are thermally stable only until the temperatures at which the damages are annealed out [198]. This should not happen at the device operating temperatures. In general, sheet resistance of damage-related implant isolation is a function of the post annealing temperature. The initial sheet resistance can be several orders of magnitude higher than unimplanted value. With annealing, the sheet resistance can be improved. It rises with increasing temperature, until a maximum value is reached. This rise depends on the implant dose. With high enough dose, before annealing all of the carriers are trapped but high concentration of damage sites makes it possible for carriers to hop from one site to the another free site. As the material is annealed the damage trap density is reduced, bringing it closer to carrier density, which prevents hopping and resistivity reaches maximum value. Further increase in annealing temperature, reduces the trap density below carrier concentration and resistivity drops very fast, until the original resistivity is reached [198]. Therefore, a temperature limit must be set for further processing after implantation in order for isolation to be preserved.

Some of the most commonly used ion species for isolation implantation are H^+, He^+, B^+, O^+ and Fe^+. With heavier ions smaller dose is needed to reach high resistivity. However, they also have shorter projected range, requiring higher energies for deeper implantation. Proton (H^+) implantation is most widely used in photonic III-V device fabrication. As the lightest ion, it can penetrate furthest, however the temperature stability of isolation regions created by proton implantation is poorer as damages may get annealed out at lower temperatures [198].

The effectiveness of the implant isolation varies with different materials, depending on their energy band structure. It can be very effective in GaAs-based compounds, both n- and p-type, but less so for InP-based compounds due to smaller bandgap. In n-type InP, the defects pin the Fermi level closer to the conductive band, not in the middle, making it easier for electrons to escape, which limits the maximum resistivity that can be reached. Also, the damages are completely annealed at temperatures as low as 300 °C [199]. p-type InP can reach higher resistance as the trap levels are in the middle, but it depends on the dose, as too high dose can turn material into n-type as damage-induced defects act as donors [198]. Isolation in p-type InP is stable until annealing temperatures above 450 °C.

The TJ of epitaxy most used in this work is comprised of 30 nm p^+-InAlAs and 30 nm n^+-InP layers. Because of high doping, the implant dose should be high. Due to lower thermal stability of implanted n-InP, it is expected that damages in this layer will unavoidably be recovered during further processing. Therefore, the implantation condition is optimized for achieving high resistance in p^+-InAlAs layer. InAlAs behaves more similar to GaAs, with better stability and higher resistances possible. Unlike with p-InP, the dose is not so critical and would not lower the resistance

if too high. Damages in layers above the TJ are expected to be annealed during fabrication since some of the processes, like PECVD deposition and ohmic contact alloying, are done above 300 °C.

Implantation condition

The most important parameters for ion implantation are the energy of the ions, which determines how deep the implanted ions will penetrate into the targeted material, and the dose or fluence of the ions, which is the total number of ions implanted per unit area of the surface of the targeted material.

As the ions penetrate the target material, they loose kinetic energy through inelastic collisions with bound electrons (electronic stopping) and elastic collisions with atom nuclei (nuclear stopping). The nuclear stopping is the one that is responsible for creation of defects. The stopping process is stochastic and profile of implanted ions and generated damages will have a certain distribution over the depth of the target. Average penetration depth of the implanted ions is called projected range, and standard deviation is called longitudinal straggle. The ions will also spread laterally, which can be described by lateral straggle.

The software SRIM (Stopping and Range of Ions in Matter) can be used for simulating the implantation process [200]. The distribution of the implanted ions, and crated vacancies, can be assessed using simulation program TRIM (the Transport of Ions in Matter) which is part of SRIM. It uses Monte Carlo simulation method to simulate the collisions based on the binary collisions approximation. The input parameters are ion species, energy and implantation angle, as well as the target structure (material atomic composition and thickness).

SRIM was used to estimate the energy needed for implantation so that the vacancies have highest level in the TJ p^+-layer of the epitaxy. The full epitaxial structure (detailed description of the epitaxy will be given in the next chapter) is defined in the software and the protons are launched at an angle of 7° with respect to the direction perpendicular to the III-V surface, in order to avoid the channeling effect. Simulations were done for 100 000 protons to achieve sufficiently good resolution. The optimum energy for protons was determined to be 100 keV. The resulting distribution of protons and vacancies is shown on Fig. 3.5a. It should be noted that the peak of the proton distribution is deeper than the peak of the vacancy distribution. Sharp changes are observable at the interfaces between different materials, but the overall projected range of the vacancies seems to match the depth of the TJ.

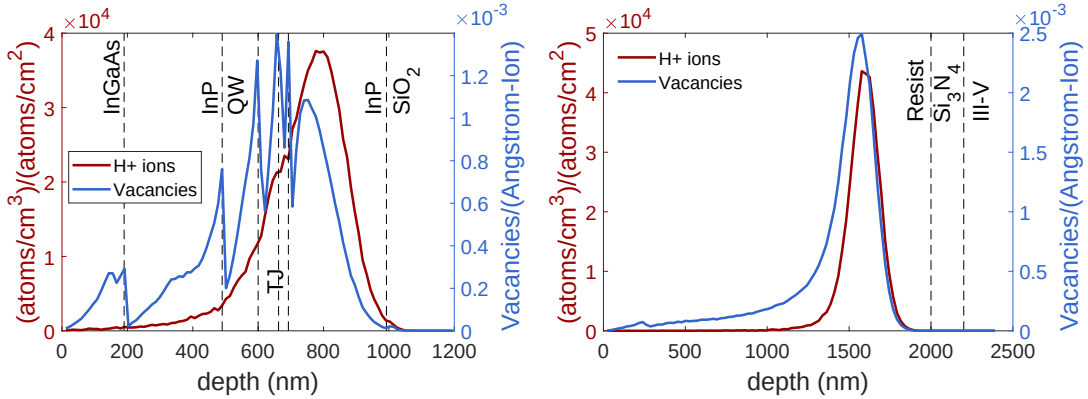


Figure 3.5: Distributions of protons and produced vacancies obtained from SRIM simulations for proton implantation with energies of 100 keV under 7° angle into (a) III-V laser epitaxy and (b) resist and SiO_2 mask. The boundaries of different layers are marked with dashed black lines.

Simulation was also done to determine the required mask thickness to protect the aperture area. As masking materials, resist, SiO_2 and Si_3N_4 were compared. For determined proton energy

of 100 keV, the projected range is 1.6 μm into the resist, 895 nm into SiO_2 and 546 nm into Si_3N_4. Since such thick SiO_2 and Si_3N_4 mask would be more difficult to fabricate, resist was chosen as a masking material. The practical thickness of the resist should be thicker than the projected range to account for lateral straggle of the distribution. However, the thicker resist would result in poorer pattern transfer during lithography. So, the resist thickness is limited to 2 um, and additional 200 nm Si_3N_4 layer is used underneath it. The pattern defined by resist was transferred to Si_3N_4 by dry etching. The proton and vacancy distribution for energy of 100 keV and angle of 7° is shown on Fig. 3.5b. The combined resist and Si_3N_4 mask completely stops the implantation of the III-V material underneath.

The implantation dose of $1 \cdot 10^{14}$ cm^2 was selected based on some of the initial tests and literature survey. Initial testing showed that higher dose leaves larger amount of damage to the layers above, leading to high series resistance that didn't get lowered enough during annealing. Longer annealing times could help improve the damage recovery, but too long exposure to temperatures above 300 °C can lead to issues with bonding in hybrid structures.

3.3.3 Undercut aperture

Selective undercut (air-gap) aperture has been considered as an alternative method of providing current guiding and confinement. It is formed by selectively wet etching a thin layer of the epitaxy, from the edge of the mesa inwards, partially until an aperture is formed in the center. The air gap prevents current flow and also provides optical index guiding. The possibility of using this method depends on the materials of the epitaxy so that only desired layers can be selectively etched.

Active layer can be etched to form the aperture [177]. However, since the active region is positioned at the standing wave peak of the optical field in the cavity, the scattering loss can be significant and together with increased sidewall recombination at the exposed facet of active region, can result in low differential quantum efficiencies. An additional sacrificial layer near the active region can be included to lower the losses [201]. By adjusting the material composition compared to active region, etching in sacrificial layer can be faster, compared to active region, so that smaller aperture is formed. The mode size would be reduced so that scattering on the larger undercut aperture in active region would be smaller. Alternatively, the materials of TJ can be chosen so that they can also be selectively etched faster than active region [202]. The advantage of creating undercut TJ aperture is that TJ is positioned at the standing wave node, so the scattering losses are reduced [194].

This method is most commonly used with InP-based lasers that use InAlGaAs QWs. The TJ can be realized using InAlAs, InAlGaAs or InP. The citric acid/hydrogen peroxide ($C_6H_8O_7$:H_2O_2) based wet etchant can be used for selective etching in this material system [203]. It etches GaAs, InGaAs, InAlAs and InAlGaAs with excellent selectivity towards InP and slow etch rate for good control of etching depth.

The active region of the epitaxy used in this work has InGaAlAs QWs, and the TJ is comprised of p^+-InAlAs and n^+-InP. The thin cladding layer between QWs and TJ is also InAlAs. Therefore, both TJ and active region will be etched without any unetched layer separating them. VCSELs with similar structure were reported in [204].

Testing undercut etching

Test etching was done to verify the possibility of using undercut aperture method. Considering limited data in literature regarding etching rate for quaternary InAlGaAs compounds, compared to InAlAs, first aim of the test was to determine the etching rate for QW and TJ layer. The portion of Al in the compound, strain and the doping levels can all influence the etch rate. It has been reported that etch rate is faster for InGaAs compared to InAlAs, so it can be assumed that etching of InAlGaAs QWs would be faster than InAlAs TJ, which is not desirable considering previous discussion.

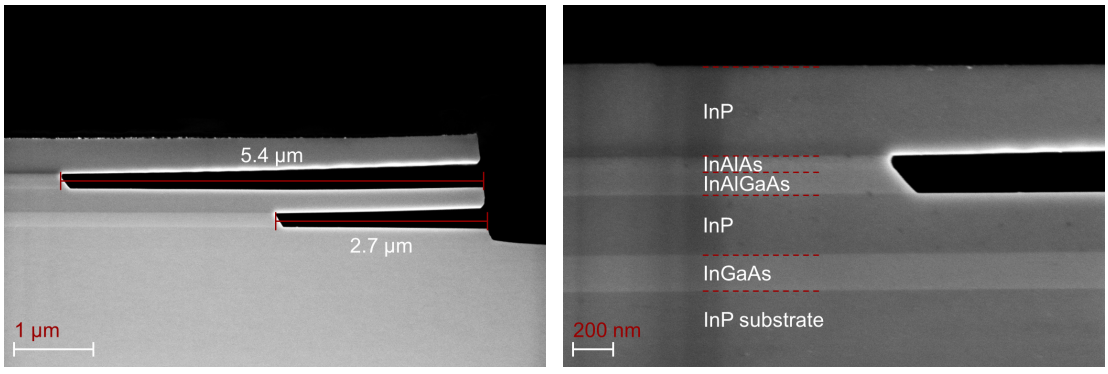
Second aim of the test is to determine the mechanical stability of free undercut structure at the desired etching depths. The thicknesses of the unetched layers and the air gap also influence the

probability of structure collapsing. Critical point drying (CPD) method needs to be used to dry the sample after wet etching to avoid collapse caused by surface tension from the liquid-to-gaseous state change during drying.

The samples of laser epitaxy were prepared by doing the mesa etching to expose the QW and TJ layers for lateral etch. Etching was done using $C_6H_8O_7$:H_2O_2 with ratio of 10:1, which gives increased selectivity to InP [203]. The etching is reaction rate limited, so the etching rate is expected to be linearly proportional to the time. The reaction rate limited etching is sensitive to the temperature, so the mixture is heated to 35 °C to enhance the etch rate and eliminate the room temperature variation. Stirring and agitation should not influence the etching, but changes in etchant mixture ratios can have drastic influence. After etching, the samples were dried using CPD and cleaved to inspect the cross-section using scaning electron microscope (SEM) to determine the etching rate

Over several etching tests, reproducibility of etching rate was very poor. For a fixed etching time of 40 minutes, the resulting etching depth varied from 7.4 μm to 21.7 μm over several repeated tests. This huge variation was attributed to the uncertainties during manual mixture preparation. For comparison, tests done using the same mixture within short time frame resulted in very similar etch depths. The rate seems to increase over time, as test repeated using same mixture after a longer time period resulted in slightly increased etching depth. This can be attributed to evaporation which changes the concentrations of the mixture components. Since no stable condition could be determined, the etching during full laser fabrication would have to be done using some sort of in situ monitoring method. The sacrificial test pillars with varying diameter could be defined during mesa patterning. As the etching progresses, the pillars with increasing diameter would be etched through and removed. Then, using optical microscope the pillars could be checked and etching depth can be determined from removed and remaining pillars.

In all tests, both InGaAlAs QWs layers and InAlAs cladding and TJ layers were etched equally to the same depth. Therefore, it is not possible to achieve different aperture sizes in TJ and active regions. Cross-section SEM image of an example of the etched structure is shown on Fig. 3.6. The sample was etched for 20 minutes after which 5.4 μm etching depth is reached. The second undercut is in the InGaAs sacrificial layer that is not part of the laser structure and is not of interest. But, it is interesting to note that etching rate is slower in InGaAs compared to InAl(Ga)As layers, which is opposite from results reported in literature. This can be attributed to influence of composition, strain and the doping, as mentioned before. The Fig. 3.6b shows the epitaxy structure and the closer look at the etched facet. The angled profile of the facet is characteristic of reaction rate limited etching process, which is anisotropic with regards to crystallographic planes [203].



(a) **(b)**

Figure 3.6: Cross-section SEM images of undercut etching done on a test sample using $C_6H_8O_7$:H_2O_2 (10:1) at 35 °C for 20 minutes. (a) Free standing structure with 5.4 μm deep etch. (b) Angled profile of the etched facet due to non-isotropic etching. Different layers of the epitaxy are labeled.

The mechanical stability of the structure is good enough. Some standing structures with air gaps as deep as 21 μm have been observed, even after cleaving for SEM inspection. However, the probability of them collapsing increases drastically with air-gap depth. Some strain present in the structure causes the bending of the free standing part upwards, which helps to prevent the collapsing but can be a problem for further processing of devices. For the air-gap depths of interest, around 8–10 μm, the probability of collapsing seems to be very low and bending is minimal, similar to example shown in Fig. 3.6a.

Due to the poor reproducibility of the etching condition and difficulty in controlling etching depth, the implantation method for current confinement has been chosen to be implemented during full laser fabrication. The undercut aperture method is left as a possibility for future work.

3.4 Ohmic contacts for InP-based lasers

Electrical current is supplied to the laser through the low resistance metal pads that are typically much larger than the laser device itself. The first critical point for the current injection is always the interface between the metal pads and the semiconductor contact layers. Poor ohmic contact can lead to high series resistance, increased heating and reliability issues. In this section the ohmic contact to n-type InP are discussed, focusing on issues that come with thin contact layers. The characterisation method will be described and experimental testing results will be given.

3.4.1 Ni/Ge/Au-based ohmic contact to n-type InP

The most widely used contact metallization for ohmic contacts to n-type GaAs and InP is Ni/Ge/Au [205]. It has some of the lowest reported values for specific contact resistance, below $10^{-6}\,\Omega\text{cm}^2$. The Ge and Au are responsible for formation of ohmic contact, while Ni improves the morphology and reliability. This metallurgy requires thermal annealing to form the ohmic contact with optimal annealing temperature around 400–420 °C. The Au and Ge are used in eutectic composition which has low eutectic temperature around 360 °C. Molten alloy allows Ge to diffuse better into III-V material where it acts as a n-type dopant, leading to highly doped region with very low energy barrier. The Au reacts with Ga or In to form the low resistance stable alloy. Ni has multiple role. It reacts with native oxide on the surface, providing better morphology and reliability of the contact. It also reacts with III-V at low temperatures, which improves the diffusion of Ge and lowers the energy required for reaction of Au with Ga or In.

Spiking issue

In this metallurgy, the reaction of Au with Ga/In is most favored one, and it would continue as long as all of Au is not spent or the thermal process is interrupted. This leads to significant diffusion of metal into the III-V material, often in form of sharp deep spikes. The poor morphology and propensity to spiking are the biggest issues with Ge/Au based contacts. The addition of Ni as first layer and use of rapid thermal annealing (RTA) can improve on these issues [205], but it can still be a problem for electrically-pumped opto-electronic devices which have very thin contact layers or are sensitive to optical losses.

In pursuit of reducing the cavity length and mode volume, the thickness of the contact layers for the lasers is kept thin to about 300 nm. Using conventional Ni/Ge/Au (30/50/250 nm) contact, issues with spiking were identified very early in this project, during initial tests of contacts and implantation conditions. The high leakage current or complete brake down of the diode I-V characteristic was observed. On occasion, I-V would change suddenly only at relatively high current levels, due to high Joules heating locally which facilitates further annealing and metal diffusion. Therefore, a solution for spiking issue was necessary for reliable ohmic contacts.

Two-step metallization approach

Alternative metallization schemes for spiking free n-type GaAs and InP ohmic contacts, based on non-alloyed contacts [205], limiting Au content[206] or replacing Au altogether [207], have been investigated. Considering that non-Au ohmic contacts usually have increased specific contact resistance, the two-step metallization approach demonstrated in [206] has been implemented.

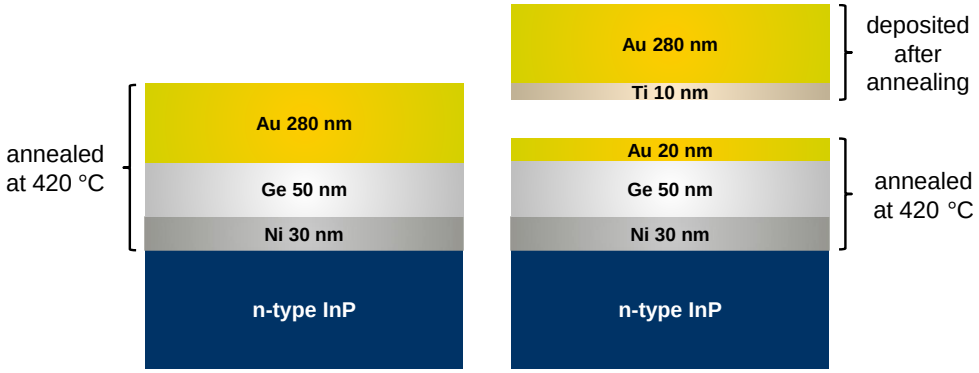


Figure 3.7: Schematic of ohmic contact structure for conventional (left) and two-step (right) approach.

Two-step approach is illustrated on Fig. 3.7. In conventional Ni/Ge/Au structure, shown on the left part of the figure, the full stack with thick layer of Au is deposited and annealed. In two-step approach, the ohmic contact is formed by Ni/Ge with as little as 30 nm of Au. Without any Au, the specific contact resistance would be significantly increased. Small amount of Au reduces the contact resistance sufficiently, while the diffusion is limited and spiking free contact can be formed. After annealing, additional thick layer of Au can be deposited to lower the sheet resistance of the contact and enable probing. Thin layer of Ti is deposited first to ensure good adhesion and to block further diffusion of Au.

3.4.2 Transmission line method

A figure of merit for the quality of the ohmic contacts to semiconductors is the specific contact resistance ρ_c, defined as resistance of a unit area of the interface between bulk metal and semiconductor. The specific contact resistance cannot be measured directly but it can be determined using transmission line method (TLM) [208].

TLM is a method to determine the contact resistance and sheet resistance of the semiconductor by measuring the dependence of the resistance versus the length of the semiconductor between two ohmic contacts. A linear array of contacts that is used for such measurement is illustrated on Fig. 3.8. Identical contacts with width W are fabricated on semiconductor with uniform doping. Mesa etching (or some other method of current confinement) is necessary to avoid current spreading outside the area between contacts.

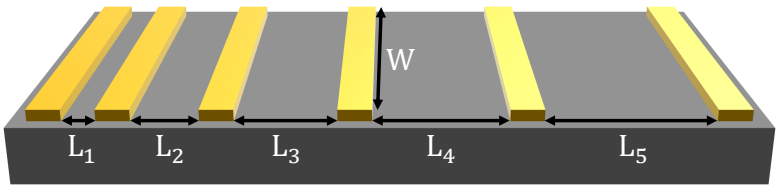


Figure 3.8: Schematic illustration of linear array of contacts for TLM measurement.

Resistance is measured between each pair of contacts with increasing distance L_i. The resistance of the resistor depends linearly on its length:

$$R = R_{sh}\frac{L}{W}, \tag{3.3}$$

where R_{sh} is sheet resistance, W is the width and L is the length of the semiconductor. Therefore, for good ohmic contacts, the results of TLM measurement should follow a simple linear model:

$$R_T = 2R_c + R_{sh}\frac{L}{W}, \tag{3.4}$$

where R_c is contact resistance of metal/semiconductor interface. By doing a linear fit of data, as illustrated on Fig. 3.9, the R_c is determined from the intercept with y-axis and R_{sh} is determined from the slope. The current flow from and into contacts is not uniform. The current density will be

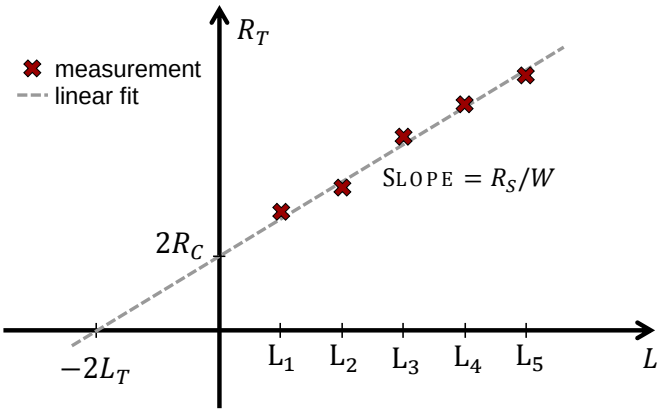


Figure 3.9: Graph of measured resistivity versus distance between contacts used to obtain specific contact resistance.

highest at the edge of the contact and it drops off away from the edge. The extent of this "current crowding" depends on the sheet resistance of the semiconductor and the specific contact resistance of the metal/semiconductor interface. Current density drop off can be approximated as

$$J(x) \sim e^{(-x/L_T)}, \tag{3.5}$$

where L_T is called transfer length, which can be defined using the specific contact resistance ρ_c as

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}}. \tag{3.6}$$

The contact resistance can then be written as

$$R_c = R_{sh}\frac{L_T}{W} = \frac{\rho_c}{L_T W}. \tag{3.7}$$

If we insert this result into Eq. (3.4), we get:

$$R_T = \frac{R_{sh}}{W}(L + 2L_T). \tag{3.8}$$

It can be concluded that L_T can also be determined from the TLM measurement as the projected intercept of the linear fit with the x-axis, as illustrated on Fig. 3.9. Then, specific contact resistance can easily be obtained from Eq. (3.7).

3.4.3 Ohmic contact testing

The implementation of ohmic contacts formed using metallization scheme introduced in section 3.4.1 has been investigated. Simple large light-emitting diodes (LEDs) are fabricated from the laser epitaxy with TJ and thin contact layers to test the current injection and verify that no spiking occurs during thermal annealing. Due to TJ, both contacts are n-type and can be fabricated together. Ohmic behavior and specific contact resistance are investigated using TLM.

Fig. 3.10 shows the measured voltage-current (V-I) characteristic of a fabricated LED device. Typical diode characteristic is observed, with no current leakage that would be evidence of deep spiking from top ohmic contact. Strong spontaneous emission is captured with infrared (IR) camera, as shown in inset of the figure.

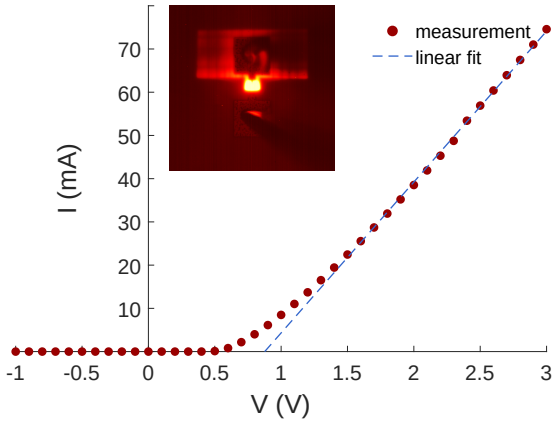


Figure 3.10: V-I diode characteristic of a LED device. The inset shows the IR camera image of the light emission from the LED at 2.5 V.

An example of fabricated TLM structure is shown on Fig. 3.11. In the image the III-V mesa is narrow grey area. The ohmic contacts are deposited and patterned with very narrow margin ($< 1\,\mu$m) from the edges of the mesa to avoid current spreading for accurate measurement. The mesa width is designed to be $15\,\mu$m or $21\,\mu$m and contact width is $13\,\mu$m or $19\,\mu$m, respectively. The lateral length of the contact is $5\,\mu$m. The distances between contacts are increments of $10\,\mu$m. Contact pads with thick Au are deposited in second metallization step after planarizing the structure with BCB polymer. The pads extend from the ohmic contacts over the BCB to increase the area for easier probing. The metal that lies on top of BCB is darker in color due to roughness of the etched BCB surface.

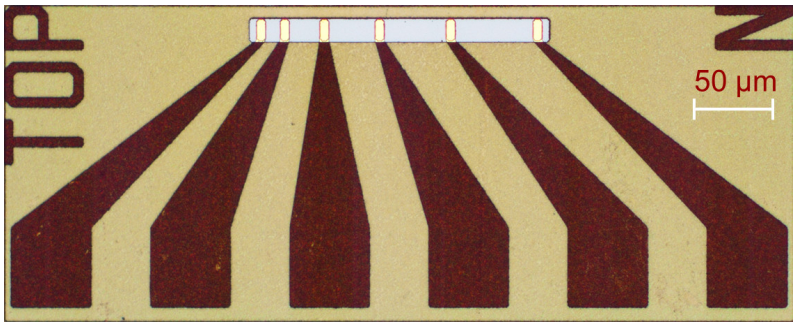


Figure 3.11: Microscope image of fabricated TLM structure.

In the first test, the contacts showed proper ohmic behavior, with linear trend from TLM measurement. However, the specific contact resistance was derived to be $7.6 \times 10^{-5}\,\Omega\text{cm}^2$, more than an order of magnitude higher than state of the art values reported in literature which are

typically lower than $10^{-6}\,\Omega\text{cm}^2$ [206]. This is attributed to unoptimized annealing process. By using better optimized RTA process for contact annealing, the specific contact resistance improved. On average, specific contact resistance in following samples was around $1.1 \times 10^{-6}\,\Omega\text{cm}^2$, with best values measured to be as low as $6.6 \times 10^{-7}\,\Omega\text{cm}^2$, matching the previously reported best values. The Fig. 3.12 shows an example of one TLM measurement. Linear V-I characteristic shows good ohmic behavior, with resistances increasing linearly with distance between contacts.

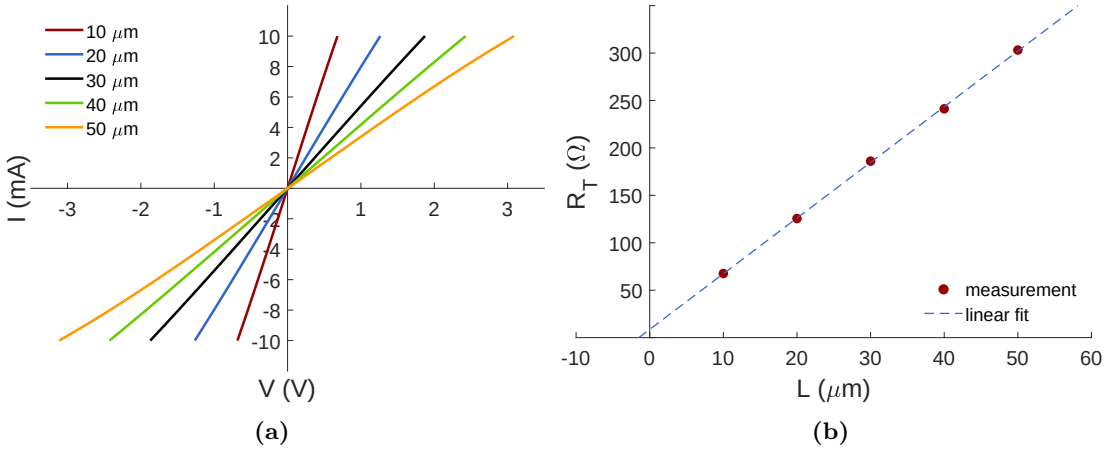


Figure 3.12: Example of TLM measurement results. (a) V-I measurement for different distances between contact. (b) Resistance versus distance, with linear fit.

3.5 Summary

In this chapter a closer look is taken into some of the difficulties when it comes to electrical pumping of VCSELs and how the electrical phenomena influence the performance.

Extrinsic parasitic response is described as a low-pass filter function that lowers the total modulation response and reduces the possible 3-dB bandwidth of the laser. The parasitic cut-off frequency depends on the parasitic elements of the whole laser.

Various parasitic resistances and capacitances of a VCSEL are identified and discussed. Using tunnel junction, the *p*-type contact layers can be avoided which helps to reduce the series resistance of the diode. By reducing the mesa size, the parasitic capacitance can be reduced.

A short overview of some of the most successful current confinement methods in VCSELs is given. Oxide apertures and buried tunnel junction demonstrated some of the best performance, however they were not applicable for this project. As an alternative, proton implantation and selective undercut etching aperture methods are investigated. Creation of aperture using implant isolation is discussed to identify the best approach for given epitaxy design. Implantation is simulated to determine the optimum parameters to implant the *p*-side of the tunnel junction. Undercut etching has been experimentally investigated. It was challenging to establish a reproducible etching condition and it was determined that it is not possible to selectively etch tunnel junction layer without etching the active region equally. This would lead to larger optical losses and degrade the differential quantum efficiency of the laser. Therefore, the undercut method was not implemented in full laser designs in this work, focusing primarily on implantation for current confinement.

Finally, ohmic contacts are considered. During early testing with conventional metallization, issue with spiking was observed. A two-step metallization approach is implemented to avoid this issue. This method is based on low-Au metallization, which limits the diffusion of Au during thermal annealing. Testing was done to verify that spiking is not happening and specific contact resistance is tested using described transmission line method measurements.

CHAPTER 4

Device designs

4.1 Introduction

The optical design of the VCSELs investigated in this work has been presented and explained in chapter 2. Theoretical background of the all design choices and how they lead to high performance has been discussed. In chapter 3 the focus was on electrical pumping issues. Methods and designs for reducing parasitics and improving carrier confinement have been discussed. In this chapter, it all comes together and the specific designs that have been fabricated and characterized will be presented. First, the general targeted VCSEL design will be presented in more detail. Then, four variations of the design, with different epitaxies or geometry will be given in detail.

4.2 Hybrid VCSEL design

The simplified schematic illustration of the chosen optical design of hybrid VCSEL structure was shown on Fig. 2.18. The general target structure is summarized in Table 4.1. It can be separated in three parts: the deposited DBR, the III-V epitaxy and the Si substrate. The DBR is dielectric, made by depositing three to four pairs of $\lambda/4$ SiO_2 and a-Si layers. If the epitaxy structure is found to deviate from the design, additional layer of SiO_2 and/or a-Si is used to fine tune the phase matching condition. The III-V epitaxy is designed for intra-cavity contacts, and it features four key parts: top contact layer, QWs as active region, tunnel junction, and bottom contact layer.

Table 4.1: Structure of hybrid VCSEL.

Material	Period	Function
SiO_2/a-Si	3–4	Dielectric DBR
InP		Top contact layer
QW	5–7	Quantum wells
TJ		Tunnel junction
InP		Bottom contact layer
SiO_2		Dummy cavity layer
BCB		Bonding layer
Si		Grating layer
SiO_2		BOX
Si		Substrate

Table 4.2: Structure of SOI wafer.

Material	Thickness (μm)	Function
Si	0.480	Device layer
SiO_2	1	BOX
Si	575	Substrate

For n-type contacts, InP is the material of the contact layers. The QWs are strained and target emission is in 1.55 μm range. The TJ is highly doped pair of p^+ and n^+ layers that is separated from the QWs by a thin cladding layer, so that the TJ falls at the node of the optical field standing wave for minimum loses. The cavity length is targeted to be 2λ long. Several different epitaxies have been used, and more details will be given in following sections. The III-V epitaxy is bonded to a SOI and InP substrate is etched away to form the hybrid III-V-on-Si structure. The SOI is comprised of 480 nm Si device layer and 1 μm BOX, as specified in Table 4.2. The same SOI structure is used for all fabricated designs in this work. HCG is defined in Si device layer of the SOI, and the BOX layer acts as low-refractive-index material below the grating. A layer of SiO_2 is sandwiched between the III-V epitaxy and Si to act as low-refractive-index material above the grating. Compared with previously published optically-pumped demonstration which uses air gap, silica is chosen due to easier fabrication and better reliability and stability, even though it results in slightly thicker layer. Since this layer is part of the resonator, its thickness needs to be optimized also for targeted cavity length and wavelength. Finally, a thin polymer layer of 30 nm BCB is used for adhesive bonding of III-V to SOI, which will be explained in detail in chapter 5.

The devices are separated by etching all the way through the III-V layers to form isolated mesas. The mesa size is designed to be as small as possible, depending on the targeted mode size and considering the fabrication alignment tolerances. This is done with goal of creating an air-post structure, for tighter optical and carrier confinement, and to reduce the parasitic capacitance. A second partial mesa etch is used to expose the bottom contact layer. Thanks to the TJ, both contacts are n-type and can be fabricated at the same time. The structure is planarized with dielectric on which large-area contact pads are sitting. The DBR is patterned into small mesas, depending on targeted mode size.

4.3 Design versions

Four different versions of VCSELs, regarding the geometry, epitaxy and current confinement have been investigated. The summary of all versions is given in Table 4.3. The versions are labeled V1–V4, and this notation will be used throughout the rest of the thesis. All dimensions are function of target mode size, which range from 5 μm to 13 μm and are defined by the heterograting well size.

The epitaxies have not been grown in-house. The designs of active region and tunnel junction have not been investigated in this work. The epitaxies were ordered from other research groups or companies who were responsible for active region and TJ designs.

Table 4.3: Summary of design versions.

Version	Epitaxy	Current confinement	Geometry	Contacts layout
V1	TJ1	Implantation	Symmetric	Ring contacts
V2	TJ2	Implantation	Asymmetric	Parallel contacts
V3	TJ2	Air-post	Asymmetric	Parallel contacts
V4	PIN	Air-post	Asymmetric	Parallel contacts

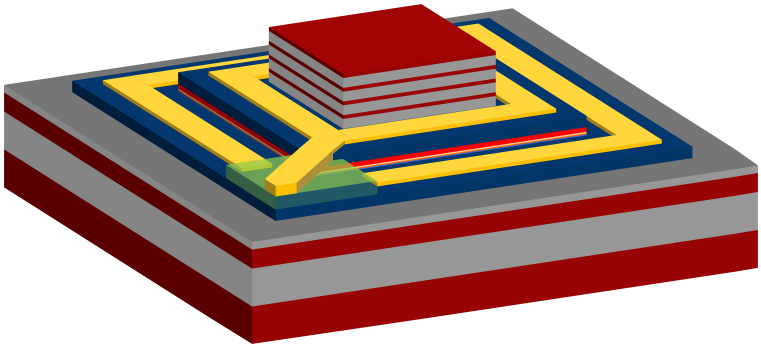


Figure 4.1: Illustration of v1 VCSEL. The dark red color is Si, grey is SiO_2, dark blue is InP with bright red active region, yellow are the metal contacts and green is the Si_3N_4. The grating is not visible as it is covered by III-V mesa. The contact pads are not included in the illustration.

4.3.1 v1 VCSEL

The design of the first version of VCSEL is illustrated on Fig. 4.1. The design of the mesa geometry is symmetrical, with second mesa centrally positioned relative to first mesa. The contacts are designed in ring shape, with top contact surrounding DBR and bottom contact surrounding second mesa. The width of the ohmic contacts is 3 μm, and 2 μm spacing is left between the mesa edges and the contacts for misalignment tolerance. So, the second mesa is 7 μm smaller than first mesa from all sides. The top contact pad is connected with top ohmic contact with narrow segment which is lifted and isolated from bottom contact layer by silicon nitride (Si_3N_4) layer (shown in green on the figure) which is used in this version to planarize the structure.

The epitaxy labeled TJ1 is used for this version of the VCSEL, and detailed structure is given in Table 4.4. It uses InGaAs/InAlGaAs tunnel junction, highly doped to $10^{20}\,cm^{-3}$ level. The active region consists of 5 strained quantum wells based on InGaAsP compounds. Undoped InP

Table 4.4: Structure of TJ1 III-V epitaxy.

Material	Thickness (nm)	Doping (cm^{-3})	Period	Function
InGaAs	20	undoped		Protective cap layer
InP	334	n-type (2×10^{18})		Bottom contact layer
InGaAs	20	n-type (1×10^{20})		TJ (n^+)
InAlGaAs	10	p-type (1×10^{20})		TJ (p^+)
InP	60	undoped		Lower Spacer
InGaAsP	7.5	undoped		Barrier (tensile strain)
InGaAsP	7.5	undoped	5	Well (compressive strain)
InGaAsP	7.5	undoped	5	Barrier (tensile strain)
InP	150	undoped		Upper spacer
InP	290	n-type (2×10^{18})		Top contact layer
InGaAs	250	undoped		Etch stop layer
InP	350 μm	n-type		Substrate

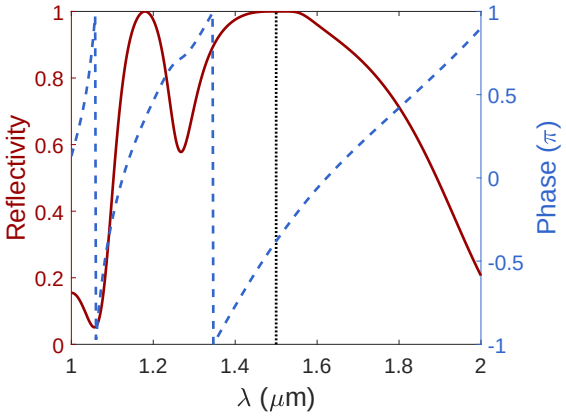


Figure 4.2: Reflectivity spectrum and phase of HCG optimized for 1.5 μm for design with TJ1 epitaxy. The black dotted line marks target wavelength.

spacer layers are used for current spreading. The total thickness of cavity layers is only 2λ, thanks to very thin contact layers. The first grown 250 nm InGaAs layer is used as etch stop layer during substrate removal. It is not part of the cavity and is removed during fabrication. The last grown is 20 nm InGaAs protective cap layer, which is removed before the III-V sample is bonded with SOI.

While targeted wavelength for peak gain of the active region is supposed to be 1.55 μm, the photoluminescense (PL) measurements of the wafers showed that peak gain is located around 1.48–1.5 μm. Therefore, the HCG parameters, DBR layer thicknesses and SiO_2 dummy cavity layer thickness have been readjusted targeting at 1.5 μm lasing. The grating is located in the center of the mesa, and its period Λ is 676 nm and bar width is 320 nm. The calculated reflectivity spectrum and reflection phase of such HCG is shown on Fig. 4.2. At targeted wavelength, the calculated reflectivity is $> 99.99\%$. The heterograting well dimensions are designed to match target mode size, and barriers are made by reducing the grating bar width by 10 nm at every Λ step outside the well. The dummy silica cavity layer above the grating needs to be 184 nm.

Both undercut etching and proton implantation were considered as current confinement methods for this structure. Due to symmetrical design, lateral etching can be done from all sides to create aperture positioned exactly in the center of the mesa where cavity is formed. Even though the lithography mask for this process was designed, the undercut etching method was not used, as discussed previously. The proton implantation was implemented and aperture is defined simply by masking the area with desired aperture size in the center of the mesa where the cavity is formed.

4.3.2 v2 VCSEL

Some of the issues with v1 design were identified during the fabrication and characterization. Patterning of narrow 3 μm contacts was a challenge. Being close to the limit of lithography resolution made edges of the pattern poor and tight alignment tolerance made it likely for bottom contact to touch the second mesa sidewall. Isolation with Si_3N_4 for top contact pad was not sufficiently thick in some batches, so current leakage was observed. The mesa sizes were relatively large, to accommodate contacts from all sides, leading to potentially increased capacitance.

VCSELs were redesigned for next version to address these issues. The contacting scheme is simplified and mesa size is reduced. The new design is illustrated on Figs. 4.3 and 4.4. The second mesa is made asymmetrically, so that bottom contact layer is opened only on one side of the device. The top and bottom contacts are placed parallel on opposite sides of the device. Top contact is 5 μm wide and bottom contact is 10 μm wide. Top contact width is smaller to keep the mesa size as small as possible for smaller device capacitance. The bottom contact has less effect on capacitance, so it is made larger to reduce series resistance. The spacing between contact and mesa sidewall is increased to improve tolerance to misalignment. BCB polymer is used for planarization in this

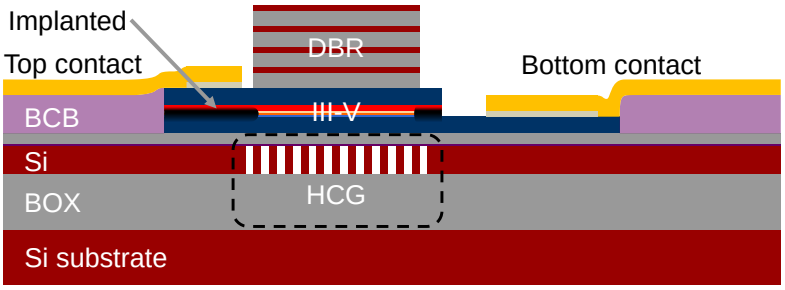


Figure 4.3: Detailed schematic cross-sectional illustration of v2 VCSEL, showing the asymmetric design of contacts and implant aperture. The color scheme is the same as on Fig. 4.1.

design. Due to parallel arrangement of contacts, there is no overlap of contact pads and opposite contact layers. The sufficient height of the BCB surface to cover the sidewalls of active region and TJ can be achieve more easily. This structure design, with minor modifications, is also used for v3 and v4 designs.

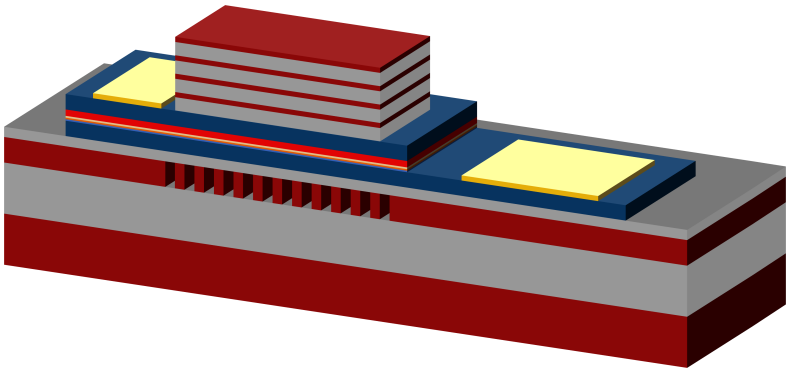


Figure 4.4: Illustration of v2 VCSEL showing one half of the device cut down the middle. The color scheme is the same as on Fig. 4.1. Planarizing polymer and contact pads are not included in illustration.

The epitaxy labeled TJ2 is used for this version of the VCSEL, and detailed structure is given in Table 4.5. It features slightly thicker InAlAs/InP tunnel junction, doped to $10^{19}\,\mathrm{cm}^{-3}$ level, which is less than in TJ1. The 7 quantum wells, based on InGaAlAs compounds, act as the active region. The spacer layer between QWs and TJ is only 35 nm in TJ2 and is made of undoped InAlAs. The epitaxy was originally grown for a different design, and total cavity thickness was not appropriate for targeted design in this work. To solve this, epitaxy is modified by etching around 132 nm of bottom contact layer before bonding.

The peak gain of TJ2 epitaxy is located around 1.545 μm, and the design is optimized for same wavelength. The HCG period is the same as in previous design, $\Lambda = 676\,\mathrm{nm}$, but the bar width is increased to 345 nm. The calculated reflectivity spectrum and reflection phase of such HCG is shown on Fig. 4.5. At targeted wavelength, the calculated reflectivity is $> 99.97\%$. The heterograting barriers are made by increasing the grating bar width by 4 nm at every Λ step. The dummy silica cavity layer above the grating is 200 nm in this design.

Proton implantation is used in this design for defining current aperture, and implanted region is illustrated on Fig. 4.3. Current must travel laterally to reach the area where resonator is formed.

Table 4.5: Structure of TJ2 III-V epitaxy.

Material	Thickness (nm)	Doping (cm^{-3})	Period	Function
InGaAs	20	undoped		Protective cap layer
InP	435	n-type (1.5×10^{18})		Bottom contact layer
InP	30	n-type (2×10^{19})		TJ (n^+)
InAlAs	30	p-type (2×10^{19})		TJ (p^+)
InAlAs	35	undoped		Cladding
InGaAlAs	7.5	undoped		Barrier (tensile strain)
InGaAlAs	6.5	undoped	7	Well (compressive strain)
InGaAlAs	7.5	undoped	7	Barrier (tensile strain)
InP	300	n-type (1.5×10^{18})		Top contact layer
InGaAs	190	undoped		Etch stop layer
InP	350 μm	n-type		Substrate

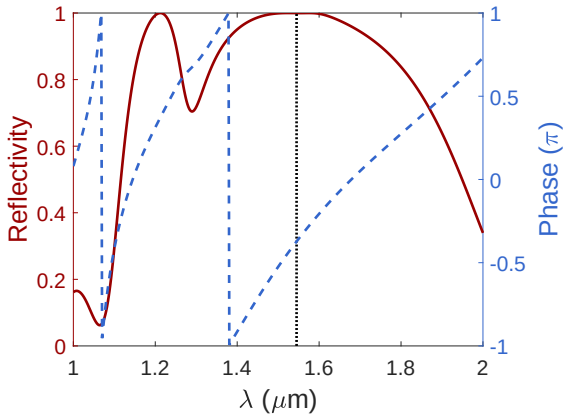


Figure 4.5: Reflectivity spectrum and phase of HCG optimized for 1.545 μm for design with TJ2 epitaxy. The black dotted line marks target wavelength.

4.3.3 v3 VCSEL

To test possible issue with aperture formed by implant isolation, which will be discussed in chapter 7, v3 VCSEL design without aperture was created and tested. The v3 design is based on v2 design and keeps the same contact design, epitaxy, resonator design and similar asymmetric layout. However, to address the lack of aperture, mesa sizes are further reduced to improve current confinement of the air-post structure. For the same targeted mode size (grating well size) v3 mesas are 6 μm narrower compared to v2. The spacing between bottom contact and second mesa edge is also reduced. The current will inevitably, to some extent, flow directly down below the top contact outside of resonator area, which would result in decreased transverse confinement factor and increase in threshold current.

4.3.4 v4 VCSEL

For v4 VCSEL, a PIN diode structure without TJ is investigated, aiming to demonstrate the lasing from the proposed VCSEL design, without pushing the design for high-speed operation.

Table 4.6: Structure of PIN III-V epitaxy.

Material	Thickness (nm)	Doping (cm^{-3})	Period	Function
InP	20	undoped		Protective cap layer
InGaAsP	20	undoped		Protective cap layer
InP	617	n-type (1.5×10^{18})		n contact layer
InP	43	n-type (5×10^{17})		Current blocking
InGaAlAs	9	undoped		Barrier (tensile strain)
InGaAlAs	7	undoped	7	Well (compressive strain)
InGaAlAs	9	undoped	7	Barrier (tensile strain)
InAlAs	100	p-type (5×10^{17})		Current blocking
InP	43	p-type (5×10^{17})		Current blocking
InP	263	p-type (1.5×10^{18})		Cladding layer
InGaAs	200	p-type (5×10^{18})		p contact layer
InP	25	undoped		Etch stop layer
InGaAs	250	undoped		Etch stop layer
InP	350 μm	n-type		Substrate

New epitaxy, labeled PIN, was obtained for this version. The detailed structure is given in Table 4.6. The active region is again comprised of 7 InGaAlAs QWs. The PL measurement showed that gain peak is positioned around 1.535 μm. Low doped current blocking layers and thicker contact layers help with lateral current spreading. Bottom contact is n-type InP, while p-type contact layer is InGaAs which has higher carrier mobility and lower resistance.

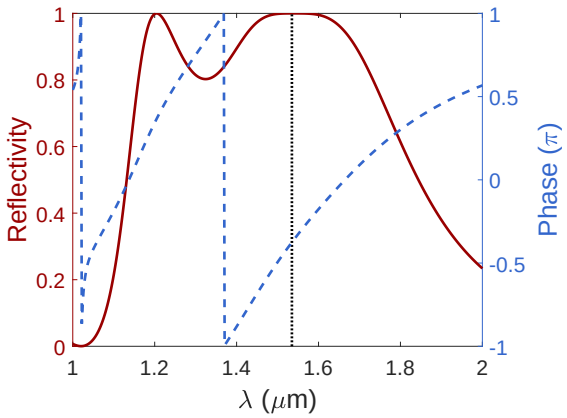


Figure 4.6: Reflectivity spectrum and phase of HCG optimized for 1.535 μm for design with PIN epitaxy. The black dotted line marks target wavelength.

The design used for V4 is the same as used for V3, with compact air-post structure and no aperture. Since InGaAs is absorbing at the targeted lasing wavelength, the top contact layer is selectively removed in area where resonator is formed. The HCG parameters are adjusted for target wavelength of 1535 nm, with period of 672 nm and grating bar width 340 nm. The calculated reflectivity spectrum and reflection phase of such HCG is shown on Fig. 4.6. At targeted wavelength,

the calculated reflectivity is $> 99.99\%$. The dummy silica cavity layer above the grating is 160 nm in this design.

4.4 Summary

The hybrid VCSEL is comprised of dielectric deposited DBR, III-V epitaxy with multiple-quantum-well active region and tunnel junction, and HCG defined on SOI. Lasers are designed as air-post structures with minimized mesa sizes. Due to the nature of the mirrors that form the laser cavity, the contacts are formed as intra-cavity. Four variants of based on this design have been investigated.

The first version (V1) features symmetric mesa design and ring-shaped contacts. It uses epitaxy TJ1 with thin tunnel junction and gain peak at 1.5 μm. Proton implantation is used to create aperture for current confinement.

The second version (V2) introduces asymmetric mesa design with parallel contacts. Different epitaxy TJ2 with shorter spacing between QWs and TJ. The resonator is designed for lasing wavelength of 1.545 μm. Proton implantation is used to create aperture for current confinement.

The third version (V3) follows the same design as V2, but with more compact air-post mesa sizes and no aperture definition.

The fourth version (V4) is designed for PIN epitaxy with thicker contact layers and current blocking layers for better lateral current distribution. Same compact asymmetric air-post design as for V3 is used.

Each design is an evolution of the previous, based on the characterization results after each of them is fabricated. The motivation and reasons for each design choice will be explained in chapter 7, where characterization results of fabricated lasers will be presented.

CHAPTER 5

Wafer Bonding of III-V to SOI

5.1 Introduction

As pointed out in chapter 1, light source devices are the most difficult to realize on Si platform. Hybrid integration of III-V and Si materials seems like most efficient way to overcome this obstacle, and it can be done in several ways. Some of them were also discussed in chapter 1 regarding lasers on silicon. However, requirement for CMOS compatibility, such as limited thermal budget, contamination, planarization, etc., disqualifies some of these methods. Direct epitaxial growth could be considered the most desirable approach, however the issues with quality of grown material have still not be solved and such processing may not be CMOS-compatible. Flip-chip bonding of pre-fabricated III-V devices on Si platform also isn't CMOS-compatible due to non-planar nature of such structure and integration density is limited.

Wafer bonding is one of the most promising approaches for hybrid integration [38]. Quite a few methods for bonding two wafers have been developed. They can be grouped into bonding methods with and without intermediate layers. Anodic and direct bonding are methods that do not use any intermediate layer, relying on electro-static and molecular forces to join two wafers. Adhesive, glass frit and metal bonding methods are achieved using some kind of intermediate bonding layers, such as polymers, glass with low melting temperature or metals. For application in photonics, where III-V materials are joined with SOI, several conditions for bonding are imposed, such as the requirement for optical transparency, low thermal budget due to mismatch of coefficients of thermal expansion, CMOS compatibility, low thickness of bonding interface, etc. Direct bonding and adhesive bonding may be the most suitable methods for this application [209].

The idea of wafer bonding is that unprocessed III-V epitaxy wafer/die is placed into contact with the SOI wafer/die that can be patterned beforehand. The two samples are then loaded into a mechanical bonding tool where pressure and temperature are applied to ensure permanent bond between two wafers. The bonding methods that will be described can be done at low temperature, within CMOS thermal budget. After bonding, the III-V substrate is removed leaving the III-V epitaxy membrane on SOI which can then be processed using CMOS-compatible planar processes. Therefore, material quality is guaranteed, as the epitaxy is grown on its own lattice-matched substrate, and the integration density is limited only by the device design. For optics, the clear advantage of this method is that III-V and Si are in intimate contact, enabling easy coupling of light from one layer to another. This key property is exploited in this work.

Apart from HCG, the wafer bonding is the key technology in the proposed VCSEL design. It is also the most critical process in the fabrication. In this chapter, two wafer bonding methods pointed out above are discussed: direct and adhesive bonding. The direct bonding method was previously adapted and optimized but was not applicable for the large part of this work. The adhesive bonding method is then implemented with significantly improved yield. The challenges and optimization of adhesive bonding with ultra-thin BCB layer will be given. The complete stable procedure for bonding used to fabricate the lasers in this work will be given in detail in next chapter.

5.2 Direct wafer bonding method

Direct wafer bonding is one of the bonding methods that do not use any intermediate layer. Two wafers with flat, mirror-polished and absolutely clean surfaces are bonded only via molecular forces, so this method is also referred to as "molecular" bonding.

5.2.1 Bonding mechanism

When two wafer surfaces are brought into intimate contact, the relatively poor Van der Waals forces cause spontaneous bonding [210]. This initial bonding happens at room temperature and in normal atmosphere. While these forces can keep two wafers together, the bonding strength is not sufficient for further processing. Bonding strength is then increased by annealing the bonded wafers at high temperature. During this process covalent bonds are formed that provide exceptionally high bonding strength.

Surface chemistry of the wafers directly influences the molecular bonding. Based on the chemical groups that are present on the surface, two types of molecular bonding have been used [210]: hydrophilic and hydrophobic bonding.

Hydrophobic bonding is achieved by removing the native oxides on the surfaces of two wafers. This is usually done with HF-solutions. This leaves hydrogen- and fluorine-terminated surface. Van der Waals and or hydrogen bonds between these groups on two wafers at room temperature contact. The high-temperature annealing step leads to removal of hydrogen and formation of crystal-to-crystal (Si–Si) bonds.

Hydrophilic surface is achieved when oxide is present on the wafer surface, which is terminated by polar –OH hydroxyl groups. At room temperature, two such wafers are bonded with a few monolayers of water between them by capillary and Van der Waals forces. Again, the weak spontaneous bonding is followed by high temperature annealing which leads to removal of absorbed water and formation of strong siloxane (Si–O–Si) covalent bonds. The presence of water molecules during initial bonding and intermediate oxide layer after annealing leads to lesser sensitivity to micro roughness of the wafers for hydrophilic bonding compared to hydrophobic bonding.

In both cases the temperature required for annealing and formation of covalent bonds can be higher than 800 °C. For that reason, this method is also referred to as fusion bonding. Such temperatures are above the limit for CMOS-compatible processing and it makes it impossible to use it for heterogeneous integration of different materials (such as III-V to SOI) due to mismatch of thermal expansion coefficients. During cooling, the strain created by different expansion would cause debonding or even cracking of wafers.

Several techniques have been developed for lowering the temperature needed for molecular bonding but most often used is oxygen plasma-assisted hydrophilic bonding.

5.2.2 Oxygen plasma-assisted direct wafer bonding

Treatment with oxygen plasma for activating hydrophilic wafer surfaces can lead to lowering of the temperature needed for bonding below 400 °C [210].

The O_2 plasma treatment affects the bonding in several ways. It helps with cleaning of the surface of any hydrocarbons and water-related species. Then, it forms a thin layer of oxide which is more hydrophilic compared to native oxide. The oxide also helps with evacuation of water and other gases that are formed at the interface during annealing step. And finally it accelerates the formation of covalent bonds at lower temperatures [209–211].

The final step is to passivate the two surfaces with a high density of polar –OH hydroxyl groups by dipping two samples into the deionized (DI) water.

The inorganic-to-inorganic polymerization reactions between Si and III-V can be described with following chemical equations [211]:

$$\text{Si–OH} + \text{M–OH} \longrightarrow \text{Si–O–M} + \text{H}_2\text{O(g)}, \tag{5.1}$$

$$\text{Si} + 2\text{H}_2\text{O} \longrightarrow \text{SiO}_2 + 2\text{H}_2\text{(g)}, \tag{5.2}$$

where M are the elements of the III-V compound. In first equation describes the process of forming covalent bonds from two weakly bonded –OH hydroxyl groups. The byproduct of this reaction is water in gaseous state. In second reaction, some of the water reacts with Si to form additional SiO_2 at the interface, with H_2 gas as a byproduct.

Oxygen plasma treatment is usually done using a reactive ion etching (RIE) process. The power of RF generator is kept relatively low to avoid physical etch of the semiconductor.

The annealing temperature is reduced significantly for plasma-assisted bonding. Usually temperature is around 300 °C [211], however bonding with even lower temperatures has been reported. Thanks to this oxygen plasma-assisted direct wafer bonding can be considered CMOS-compatible.

One issue with low temperature bonding is the outgassing of byproducts of the reaction, H_2O and H_2. The formation of these gases can lead to high pressure locally in the bonding interface, which can result in formation of voids. With high temperature annealing the gases can more easily diffuse out through the micro roughness or enter porous SiO_2 medium quickly. However, at low temperatures the diffusion process is not so efficient and large amount of voids would be formed. One effective method for getting rid of the gases is to fabricate vertical outgassing channels (VOCs) in the top Si layer of the SOI. This bonding procedure was developed by researchers from the University of California - Santa Barbara (UCSB) [211]. This provides a path for the gases to migrate down into the BOX layer, which is porous and allows gases to diffuse through it. The spacing and the size of the VOCs influence the effectiveness in preventing voids. By reducing the spacing and increasing their size, the fewer voids are formed. In our experiments, 7 μm μm square patterns with spacing of 100 μm led to void free bonding. Their small size and flexibility in placing it on the sample are clear advantage of this design. To help with squeezing the byproduct gases into the VOCs, external coaxial pressure of several MPa is applied onto the stack during annealing step. The duration of annealing is also significantly reduced to as short as 1 hour.

5.2.3 Cleaning and surface roughness requirement

The biggest drawback of direct bonding is the extremely strict requirement for ultimately flat, clean, contamination-free bonding surfaces. This means that extensive and rigorous cleaning procedures and surface preparations are necessary. Any surface roughness or particle contamination would lead to unbonded areas, voids, or reduce general bonding strength and ultimately lead to complete bonding failure.

The first step in cleaning procedure is solvent cleaning process using ultrasonic cleaner. This removes any resist protective layer and large particles. The III-V epitaxy is usually protected with (one or more) cap layer that is grown last during epitaxial growth. By selectively wet etching this layer any contaminants would be lifted off.

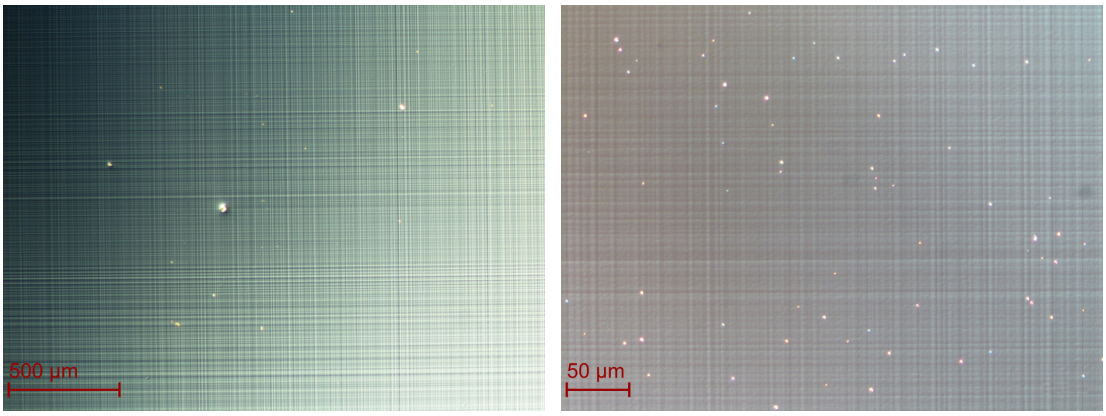
One of the commonly used rigorous cleaning methods is the RCA-1 (sometimes called "standard clean-1", SC-1) solution (1 N_4OH (95–97%) : 1 H_2O_2 (31%) : 5 H_2O) which is heated to 70–80 °C. This alkaline solution is effective for removing particles and organic materials. H_2O_2 oxidizes the wafer surface and any present particles. The NH_4OH slightly etches the wafer surface and undercuts beneath the particle, causing lift off the particle from the surface. It also causes electrical repulsion of the particle by building negative charge on the particle and the wafer surface.

The particle contamination is a big issue and requires careful handling of the samples during bonding procedure, even in high-class cleanroom environment.

Even with perfectly cleaned sample, the surface needs to be mirror-polished, flat and smooth. It is reported that micro-roughness root mean squared (RMS) should be below 1 nm [38]. Advanced chemomechanical polishing (CMP) is commonly used to achieve sufficient smoothness. In case of large structures or high density of smaller structures patterned on the wafers, they are commonly planarized with SiO_2 followed by CMP to achieve flat surface.

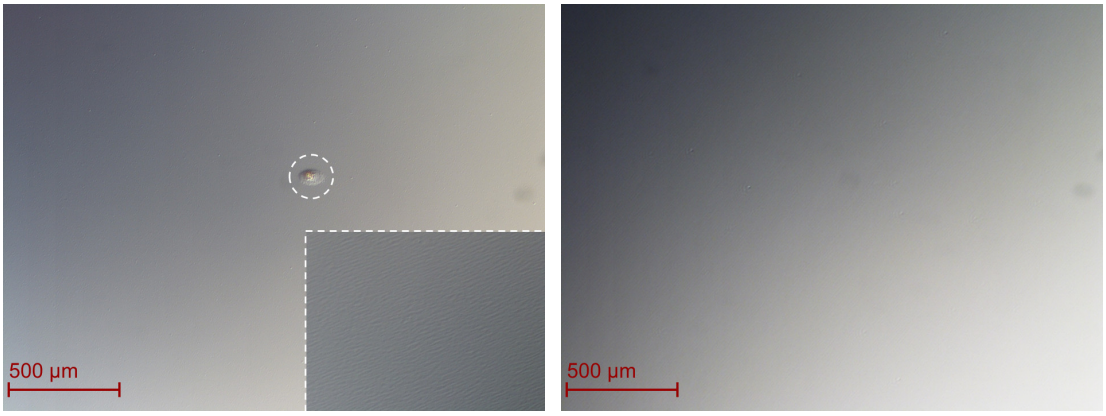
5.3 Surface roughness issue

The oxygen plasma-assisted direct wafer bonding method of III-V to SOI was previously successfully implemented and optimized in our group. It led to fabrication of optically pumped hybrid VCSELs with excellent performance [120]. This project succeeds that work and it was planned to utilize the same bonding procedure. However, from the start of the project, this method was not usable due to much poorer morphology of the III-V epitaxies designed for electrically pumped lasers. The Figs. 5.1 and 5.2 show microscope images of the surfaces of three epitaxies used in this work and described in chapter 4. The images are obtained using differential interference contrast (DIC) microscopy (also known as Nomarski interference contrast (NIC) or Nomarski microscopy) which enhances the contrast and makes particles and surface morphology more visible.



(a) **(b)**

Figure 5.1: Nomarski microscope images of the TJ2 epitaxy wafer surface. (a) Significant cross-hatch morphology [212] is noticeable on the surface along some large particles embedded during growth. (b) Closer look of another area of the wafer shows numerous smaller particles embedded into the epitaxy.



(a) **(b)**

Figure 5.2: Nomarski microscope images of the surfaces of (a) TJ1 and (b) PIN epitaxy wafers. The inset on figure (a) shows closer look at wavy surface morphology and occasional large particle is found embedded into the epitaxy during growth. The PIN epitaxy has mostly smooth surface with very rare occurrence of particles.

Both TJ1 and TJ2 epitaxies feature distinctive surface morphology. The wavy morphology is observed on the surface of TJ1 epitaxy, as shown in the inset of the Fig. 5.2a, while TJ2 has significant cross-hatch morphology [212]. Furthermore, significant amount of particles is found on both epitaxies. These particles are embedded in the epitaxy during growth process, and cannot be removed. This is particularly problem for TJ2 epitaxy, which also features high density of small particles visible at higher magnification, as shown on Fig. 5.1b. The PIN epitaxy featured significantly better surface morphology, with low amount of immovable particles and smooth surface. It is possible that higher doping concentrations required to form TJs combined with stress from the active region lead to poorer morphology of epitaxially grown layers. For that reason, PIN epitaxy and epitaxies designed for optical pumping do not suffer from such problem.

The TJ1 and TJ2 epitaxies do not fulfill the requirement for low surface roughness necessary for direct wafer bonding method. Any attempts to bond them have either failed completely or lead to debonding of large areas. This was one of the reasons that an alternative bonding method, with more relaxed requirements for surface morphology, was pursued.

5.4 BCB adhesive wafer bonding

5.4.1 Motivation

Issue with surface roughness discussed in previous section was discovered very early at the beginning of the projects, even with some of the test epitaxies for electrical pumping before final design was decided. It made the established direct wafer bonding process ineffective and it was necessary to investigate other possible methods for wafer bonding. It was clear that bonding method with intermediate layer is needed to lower the sensitivity to surface morphology. Two methods were considered: adhesive and metal bonding.

Metal Solder bonding using gold-tin (Au/Sn) eutectic alloys was shortly investigated as a potential bonding method. For the proposed design, bonding interface would be intra-cavity. Therefore, the metal layer would have to be deposited on SOI and patterned to remove metal layer in the area where optical mode would be present. Hybrid lasers using this kind of bonding method were previously reported [60]. However, the concept was ultimately found unfitting for the proposed design. Furthermore, some early testing proved that it was difficult to implement it in the cleanroom and low melting temperature of the eutectic Au/Sn alloy around 278 °C limits the thermal budget for processing after bonding.

Adhesive bonding using BCB polymer was then implemented. It offered good compromise in terms of design and fabrication requirements. Different variations of this bonding method has been previously implemented by other researchers in our department. However, the device design investigated in this work required that intermediate layer be as thin as possible. Therefore, adhesive bonding using ultra-thin BCB layers was implemented and optimized.

5.4.2 Adhesive wafer bonding

Adhesive wafer bonding is a method which relies on an intermediate layer of adhesive material to establish a bond between two wafers [213]. The adhesive fills any voids between two wafers and absorbs any morphology so that good contact is made with both bonding surfaces on molecular level. To achieve this, the adhesive is usually applied in liquid state in a process called wetting, and then force is applied to ensure the intimate contact of two wafers. Chemical bonds are then established between the adhesive and wafer surfaces when the adhesive is solidified due to the chemical transformation during curing process. This gives a permanent bond between the two wafers.

Since the adhesive is applied in some liquid form, it can easily planarize the surfaces of the wafers. It makes bonding significantly more tolerant to surface roughness or morphology. The adhesive can fill the voids and gaps, such as structures patterned on the wafers. Adhesive bonding is also tolerant to small particles and contamination, as the adhesive will envelope them so that uniform contact is still established. All this depends on the thickness of the applied adhesive layer.

Any particles or other defects that are taller than adhesive layer would still give issues. But, in any case, adhesive bonding has significant advantage over direct wafer bonding method in this regard.

Depending on the type of adhesive the hardening can be done in number of ways, e.g. by applying heat or ultraviolet (UV) light. Thermally cured adhesives are the most common and temperature required for curing process is usually lower than 300 °C.

Considering that it does not require rigorous cleaning or special wafer surface treatments it can be relatively simple process. Since it doesn't depend on the direct interaction between two wafers and with low processing temperatures, it brings possibility of joining much larger variety of materials, as long as good wetting can be done.

Despite many advantages that make adhesive bonding attractive for many applications, it also has disadvantages. It doesn't provide hermetic sealing of the interface like some of the other methods, allowing for moisture or gases to penetrate the bonded interface. It can also limit the thermal budget for processing after bonding, depending on the properties of the adhesive. Low thermal conductivity of adhesive materials can have major impact on thermal properties of the devices fabricated using this method.

5.4.3 Bonding using BCB polymer

BCB polymer as adhesive

Polymer materials are most commonly used as adhesive for bonding [213]. Wide range of polymer types, with different properties and hardening mechanism, can be used. Some of the most commonly reported bonding polymers in literature are: BCB (a thermosetting polymer), SU8 (a UV-cured polymer), polymethylmethacrylate (PMMA) and polyimides (PI) (thermoplastic polymers).

Choice of polymer depends on specific application and requirements. For application in photonics and integration of III-V and SOI, the low bonding temperature is necessary as discussed before, but polymer must offer sufficiently high thermal budget and resistance to aggressive chemicals for post-bonding processing of bonded III-V epitaxy.

Divinylsiloxane-bis-benzocyclobutene (DVS-BCB, or just BCB for short) is probably the most often used material for adhesive bonding. It was developed by Dow Chemical Company as a low dielectric constant (low-k) polymer for use as a dielectric in on-chip interconnects. Hardening of BCB occurs due to polymerization achieved by thermal curing. Some of the biggest advantages of BCB as bonding material are [214]:

- the low shrinkage and no byproducts are created during the polymerization reaction (so no voids are formed at the bonding interface),
- low curing temperature (CMOS-compatible),
- high glass transition temperature (allowing a large post-bonding thermal budget),
- excellent planarization properties.

Apart from that it has good physical properties such as [215]:

- low dielectric constant,
- low moisture absorption,
- low level of ionic contaminants,
- low optical loss ($< 0.1\,\mathrm{dB/cm}$ at $1.55\,\mu\mathrm{m}$),
- good thermal stability,
- excellent chemical resistance, etc.

The main drawback of BCB as bonding layer is low thermal conductivity which can impact the performance of devices fabricated using this technology.

It is sold commercially under name Cyclotene™ as B-staged (partially-cured) oligomer that is dissolved in mesitylene solvent. The achievable layer thickness by spin coating of the solution is determined by the amount of mesitylene solvent added and the degree of polymerization of the oligomer. It is available as both photosensitive variant (4000 series), which can be patterned using UV lithography, and non-photosensitive variant (3000 series) that is suitable for patterning with dry etching.

Adhesion promoters are commonly used to improve the adhesion of BCB to various wafer surfaces. Adhesion promoter molecules have two components: one side interacts with polymer while on other side it contains silanol groups (Si–OH) that react with free hydroxyl groups on an oxidized surface of the wafer [216]. Dow Chemicals Company commercially offers adhesion promoter for Cyclotene under name AP3000.

The degree of polymerization of BCB and its phase depends on curing time and temperature, as illustrated on Fig. 5.3. The glass transition temperature T_g increases with the increasing degree of polymerization, and BCB changes from a liquid phase (green) into a gel rubber phase (blue) and finally transforming into a solid glass phase (pink). Most commonly, practical curing is done at 250 °C for 1 hour. BCB oxidizes if exposed to oxygen during curing, which would lead to increased brittleness and cracking, so curing is performed in an oxygen-free atmosphere in the curing chamber.

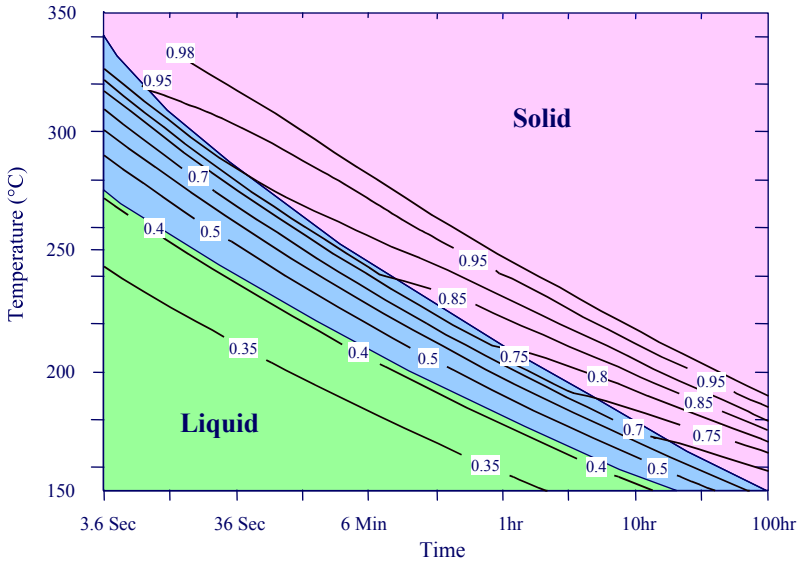


Figure 5.3: BCB polymerization and phase diagram, depending on curing time and temperature. Adapted from [217].

BCB bonding of III-V to SOI

There is little difference when it comes to bonding different combinations of wafers. Bonding of III-V samples to SOI sample is of interest for this work, therefore bonding process will be given here for that combination of materials. Photonics Research Group from Ghent University has performed pioneering work in the use of BCB bonding for this kind of heterogeneous integration and with it demonstrated various active devices on SOI platform. Probably the most significant difference that comes with use of III-V materials is that very often is done with small chips instead of wafers.

While planarizing property of BCB makes this type of bonding significantly more tolerable to uneven morphology of the surface compared to direct wafer bonding method, the surfaces should still be as clean as possible. This is especially important when bonding layer thickness is reduced to sub-micron range. Therefore, the bonding process starts with cleaning [218]. Removal of sacrificial protective layers of III-V epitaxy is effective way of cleaning III-V samples. Similar to direct bonding process, RCA-1 solution can be used to clean samples of any particles or organic materials.

After cleaning, the BCB is applied to one or both wafers [215, 218]. Usually, when bonding of small III-V chips is done, the larger SOI wafer is spin-coated as edge beads can form when small chips are spin-coated. Adhesion promoter is often spin-coated and baked first, followed by

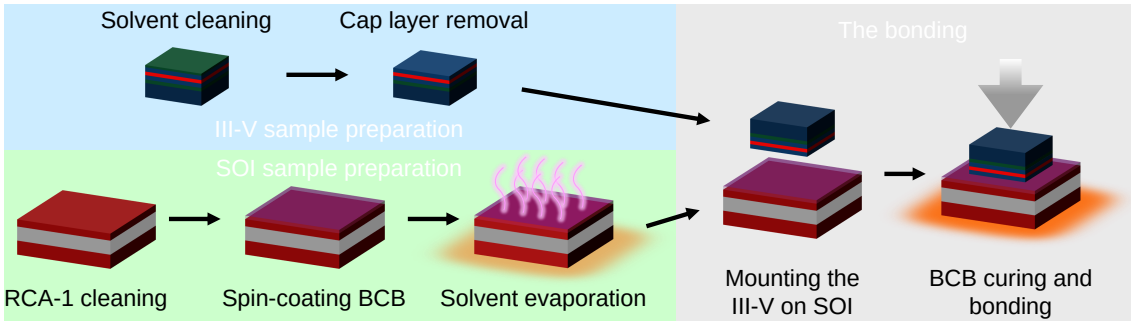


Figure 5.4: Illustration of BCB bonding procedure of III-V and SOI samples.

spin-coating of BCB itself. The short baking step is usually done to evaporate the mesitylene solvent and reflow the BCB for better planarization.

The prepared samples can be brought into contact in air or inside a vacuum environment. It is reported that contacting in air can lead to incorporation of air pockets and less reproducible results [214]. So the samples can be separated by spacers until they are loaded into the wafer bonding tool where contact is established in vacuum environment and the temperature and pressure are applied onto the stack [218]. The temperature profile usually consists of two parts: the pre-curing and hard curing. During pre-curing, the remaining solvent evaporates and BCB is still in liquid phase and can reflow and fill any voids with the help of applied pressure [218]. If pre-curing is not done, bubbles may form due to trapped solvent that evaporates with temperature increase. Too high temperature during pre-curing leads to unbonded areas where excessive curing happened before the wafers were fully bonded. Most commonly this step is done at 150 °C for 10–20 min. Next, the temperature is slowly raised to hard curing temperature (240–280 °C) where it is kept for about 1 hour, which should lead to 95–98% polymerization of BCB. After curing is finished, the sample is cooled down to room temperature and unloaded form bonding tool.

Ultra-thin BCB bonding

The thickness of BCB used for bonding reported in literature vary significantly from tens of microns to sub-micron range [214]. For application in photonics it is very often of interest to minimize the thickness of this layer, e.g. in cases where light is evanescently coupled from III-V active device into Si waveguides on SOI. For the VCL design investigated in this work, the bonding layer is part of the cavity, and therefore its thickness needs to be carefully considered.

BCB has low refractive index of 1.543 at 1.55 μm wavelength, and could act as low-refractive-index material above the grating for high reflectivity of HCG. However, it is still slightly higher than refractive index of SiO_2 (1.48), which would lower the reflectivity of the HCG and increase the required thickness. Furthermore, the thermal conductivity of BCB is almost 5 times smaller compared with SiO_2 (0.29 W/mK vs 1.4 W/mK). Therefore, it was chosen to minimize the BCB layer thickness so that main material of dummy cavity is SiO_2.

Photonics Research Group from Ghent University have been leading the research on bonding with very thin layers of BCB [218]. Keyvaninia *et al.* reported in 2013 a modification of their bonding procedure that simplified the preparation and use of bonding tool [219]. With this method, they reported successful bonding with relatively uniform BCB layer thicknesses as little as 30 nm. The ultra-thin layers of spin-coated BCB are achieved by diluting the thinnest commercial BCB solution, Cyclotene 3022-35 (with a 35% resin content) from Dow Chemical Company, with mesitylene to 1:8 ratio by volume. The spin-coated sample is pre-cured at 150 °C and then the two samples are brought into contact in open air at room temperature (compared with previously demonstrated method where samples were brought into contact inside the vacuum environment at elevated temperature). Already joined samples are then loaded into the bonding tool. Additional pre-curing is done at 150 °C for 10 min with applied pressure of up to 400 kPa, followed by a slow

increase to 280 °C for hard curing which lasts one hour.

The described bonding process seemed to fit the requirements for realization of hybrid structure for the VCSELs in this work. Therefore, experiments were done to adapt it for specifics of the proposed design and available tools in the cleanroom.

5.4.4 Bonding experiments

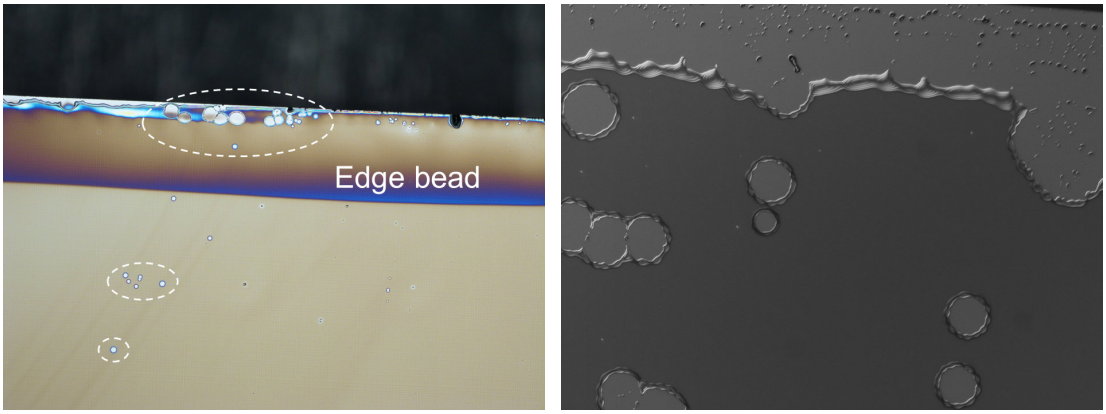
While bonding with thicker ($> 1\,\mu$m) BCB layers was routinely done by other researchers in our cleanroom, implementing of the ultra-thin BCB bonding proved challenging. With reduced thickness, the bonding became significantly more sensitive. The surface morphology seen on the III-V epitaxies could be planarized by BCB, however any particles or contamination would cause large un-bonded areas. Therefore, rigorous cleaning and careful handling was done, similar as with direct bonding procedure. Even with that, early attempts to reproduce the reported bonding results were unsuccessful.

In early testing, plain Si substrates were used, not to waste the more expensive SOI. After more stable condition was reached, the SOI was used initially without any pattern and later with pattern etched into the Si layer. RCA-1 cleaning of Si samples was done in most of the tests. Several different kinds of III-V samples were used over the course of testing. Clean InP was used for initial tests for basic bonding strength tests. However, it would not be able to give good indication if bonding is good enough for substrate removal process. Therefore, a couple of dummy epitaxies were obtained for testing that had similar surface quality as T1 and PIN shown on Fig. 5.2. Target was to obtain reliable bonding condition of TJ2 epitaxy, so testing was done with it also.

As reported in [219], Cyclotene 3022-35 was diluted with mesitylene (available as Rinse T1100 from Dow Chemical Company) in 1:8 (v/v) ratio and spin-coated at 3000 rpm for 40 s to achieve desired thickness of 30 nm. One big change was that the BCB had to be spin-coated on III-V sample, since the grating etched into the Si layer of SOI should not be filled with BCB. Two major concerns come with this change: the adhesion and uniformity. Adhesion of BCB to III-V materials is significantly poorer compared with Si or dielectric materials [216]. Initial attempts to spin-coat the sample without any adhesion layer resulted with non-uniform BCB layer. Luckily, for the device design, SiO_2 layer is required between III-V and SOI. Therefore, for test purposes thin layer ~ 15 nm of SiO_2 was always deposited on III-V after cap layer removal. This resulted improved uniformity of thin spin-coated BCB. Adhesion promoter AP3000 was also tested, but its use always resulted in appearance of voids in BCB layer, as illustrated on Fig. 5.5. Therefore, in most of the tests adhesion promoter was not used. The other big concern is formation of edge beads on the edges and especially in the corners when spin-coating a square sample. These beads can be significantly thicker and may prevent the intimate contact during bonding. For this reason, it would be advantageous to spin-coat on Si sample which is larger in size than III-V so the edge beads would be outside the bonding area. However, despite the presence of edge beads, successful bonding was achieved. It is assumed that applied pressure during pre-curing step, when temperature is such that BCB is softest, evens out the edge beads so that uniform contact is achieved.

The spin-coated III-V sample was flipped and brought into contact with Si or SOI test samples at room temperature in open air. Slight pressure is applied manually to ensure good contact. However, unlike with direct wafer bonding, the spontaneous bonding is much weaker. The dies can easily be detached with slightest force. This doesn't indicate the poor bonding, but extra care needs to be taken when loading the samples into the bonding tool to avoid movement of samples.

Testing of bonding was done using three different bonding tools. The first tool that was used in initial testing was an older model of wafer bonder from EVG (here named EVG NIL). It is parallel-plate type of bonder, where force is applied by the solid piston. The diameter of the piston head is 100 mm (equivalent to 4" wafer), however smaller sample sizes can be bonded. The surface area of bonded sample is only 7 mm × 7 mm, which is significantly smaller than minimum allowed surface in the EVG bonder. Therefore, three pairs of 2 cm × 2 cm Si samples were bonded too and arranged symmetrically on the carrier fixture around the pair of test samples that is to be bonded. The substrate thickness of these dummy support samples was chosen to match the substrate thickness of test sample. In this way the effective surface area is increased and it



(a) (b)

Figure 5.5: Microscope images of thin BCB spin-coated after adhesion promoter. (a) Large edge bead is visible at the edge of the sample and several voids in BCB layers are marked. (b) Example with more severe lack of uniformity of BCB layer due to adhesion promoter.

eliminates the requirement for strict positioning of the samples into the center for stability. Thin aluminum sheets were placed over the samples, which can deform to compensate any minor height difference between the samples.

The force applied during curing step in EVG NIL was around 1800 N, which corresponds to about 1.45 MPa pressure over the total area of the samples. Temperature is quickly increased to 150 °C and kept there for 10 min with applied force. Then the temperature is risen slowly to 280 °C for hard curing for one hour. Temperature is then brought down to room temperature and samples are unloaded form the bonding tool. InP substrate is then removed using wet etching in HCl (37%) for approximately one hour.

Several test were done using just clean InP substrates, to judge the bonding quality. They all showed good bonding strength and they didn't detach during substrate removal and were completely etched away. However, attempts to bond the rougher TJ2 epitaxy samples were unsuccessful, with III-V sample detaching before the substrate removal is finished. Therefore, different parameters of the whole process were varied in attempt to optimize the bonding strength and achieve better yield with III-V epitaxies that have less smooth surface. The temperature for hard curing was reduced to 250 °C, to reduce the stress due to thermal expansion mismatch. The tests with clean InP samples showed same results as previously, but it made no improvement of bonding of epitaxies. Change of other parameters such as baking temperature and time for solvent evaporation, moment at which the force is applied, use of adhesion promoter, changes in cleaning, etc., haven't made much improvement in stabilizing the results, with only occasional good bond.

The Fig. 5.6a shows a photograph one successful bond of and smooth dummy epitaxy and Si substrate, after the substrate is fully etched away. With rougher TJ2 epitaxy only partial success was obtained, with large parts detaching during substrate removal. The several samples with successful bonding were cleaved and BCB layer thickness is measured using SEM. The BCB layer is measured to be 30 nm with small variation (< 5 nm) over several samples. The Fig. 5.6b shows an example of SEM image of a cleaved cross-section of a bonded TJ2 epitaxy on Si substrate.

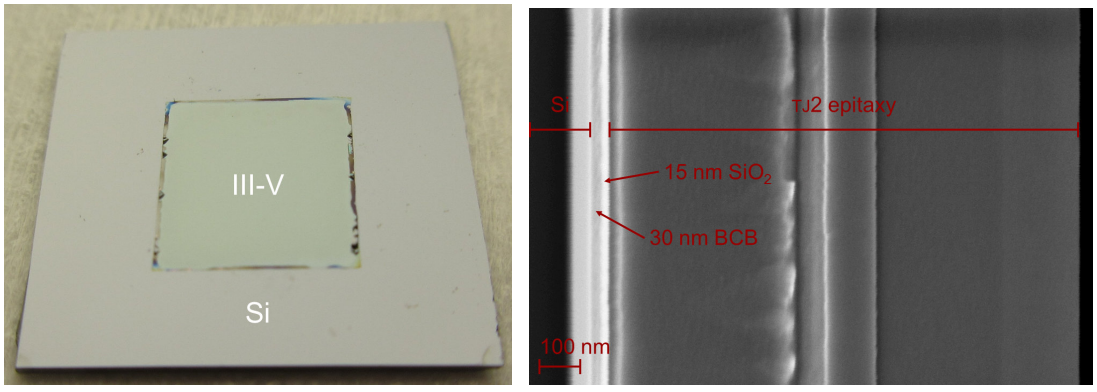
The overall bonding yield was still very low. However, before the bonding recipe could be further optimized, the EVG NIL bonding tool was decommissioned and removed from cleanroom, due to often and long braked owns and poor reliability. As a replacement the Süss MicroTec SB6 wafer bonding tool was installed and bonding process was transferred on it. This tool is also a parallel-plate type of bonder and has limited minimum sample size of 1 cm^2, and bonding of smaller pieces was allowed only using three larger support samples distributed around it, similar to previous tool. Furthermore, the allowed tool pressure in this configuration was around 130 mbar (13 kPa). Due to technical limitation, the actual lowest pressure that was measured was higher,

around 200 mbar, which resulted in measured force around 450 N or about 360 kPa over the total area of the samples. This is significant reduction compared with previous tool, but it falls within the values reported in literature [219]. The bonding optimization was continued with SB6 bonder, and high success rate was achieved with relatively smooth dummy epitaxies. One example of successful bonding of dummy epitaxy with SOI substrate is shown on Fig. 5.7.

However, bonding of TJ2 epitaxy still wasn't as good as was needed. The high density of unmovable particles present in the grown layers meant that in most of the test there was complete or partial debonding during substrate removal process. One example of successful bonding of a exceptionally clean TJ2 epitaxy with SOI substrate is shown on Fig. 5.8. Pattern was etched into the Si layer, as shown on SEM image of the cross-section, but it had no negative effect on the bonding. In this test, $\sim$ 200 nm of SiO_2 was deposited on III-V sample before the BCB is spin-coated.

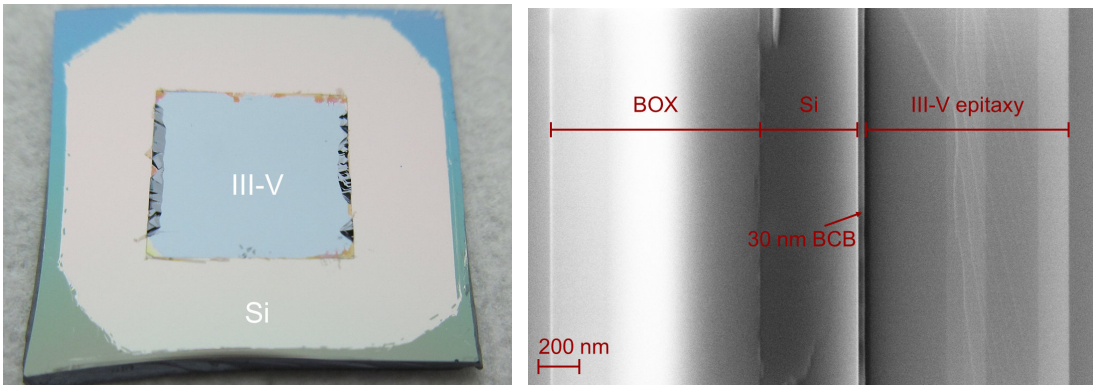
An upgrade of the SB6 wafer bonding tool led to reduction of applied tool pressure to 128 mbar (force of 225 N) and due to tool safety concerns it was not allowed to increase it again for the bonding with small sample size. With applied force cut in half compared with previous tests, all following bonding attempts were unsuccessful. For that reason, bonding was transferred to a third bonding tool.

The third bonding tool is "balloon" type that applies pressure onto the wafers via elastic membrane that is inflated inside the chamber. This type of tool is commonly used for nanoimprint lithography and hot embossing, but wafer bonding has been reported also [213, 220]. The tool that was used in this work is desktop prototype Compact Polymer Bonder (CPB) from NIL Technology, based on their commercial CNI nanoimprint tool. The small low-pressure chamber has 100 mm diameter (for 4" wafers) with a hotplate as bottom chuck and an elastic top membrane that is gas-pressurized. The maximum temperature is limited to 250 °C and membrane pressure can go up to 6 bar. Due to the elasticity of the membrane, it can conform to any shape of the samples that are placed under it for bonding. Therefore, the pressure that is applied is uniformly distributed inside the whole chamber and doesn't depend on the surface area of the sample, unlike with parallel-plate bonder where all the force is applied on the sample only. In case of parallel-plate bonder, any surface topography, tilting or asymmetry can cause the plates to not be perfectly parallel and force would not be distributed evenly over the sample area [221]. With balloon bonder, all these issues do not exist. Furthermore, the pressure uniformity is improved in case a particle is present between two wafers [221], which results in smaller unbonded areas around the particle. The pressure used for the bonding was initially set to 3 bar (300 kPa) but later increased to 4 bar (400 kPa), which is higher than what was possible with previous tool, but it didn't make any difference on the results.



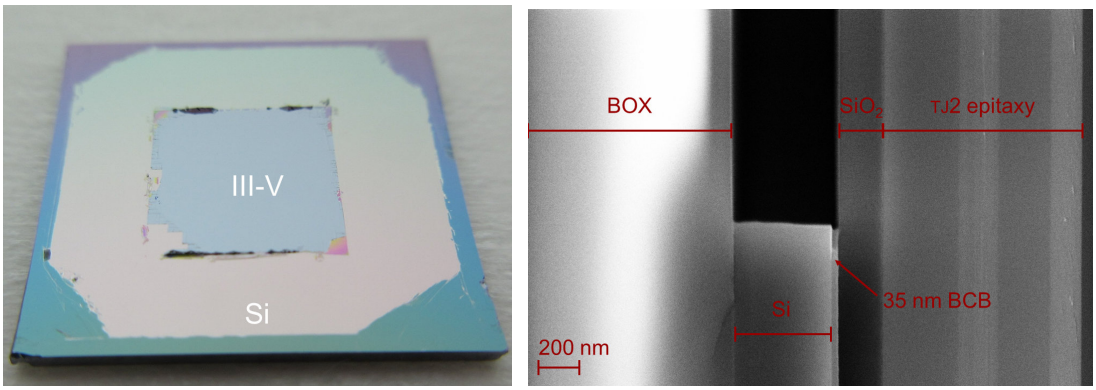
(a) **(b)**

Figure 5.6: (a) Photograph of perfectly bonded dummy epitaxy on Si substrate after substrate is removed. (b) SEM image of a cross-section of the bonded stack. 15 nm of SiO_2 is deposited on III-V epitaxy before BCB is spin-coated. Measured thickness of BCB is 30 nm.



(a) (b)

Figure 5.7: (a) Photograph of bonded dummy III-V epitaxy on SOI substrate after substrate is removed. (b) SEM image of a cross-section of the bonded stack. 15 nm of SiO_2 is deposited on III-V epitaxy before BCB is spin-coated. Measured thickness of BCB is 30 nm.



(a) (b)

Figure 5.8: (a) Photograph of bonded TJ2 epitaxy on SOI substrate after substrate is removed. (b) SEM image of a cross-section of the bonded stack with patterned Si device layer. 210 nm of SiO_2 is deposited on III-V epitaxy before BCB is spin-coated. Measured thickness of BCB is 35 nm.

The wafer bonding test done using NILT CPB gave excellent results. Successful bonding was obtained even with TJ2 epitaxy, as long as there was no large defect on the surface. After bonding with previous tools, during substrate removal, often small areas around the edges and corners would detach. With balloon bonder, the edges and corners would also remain bonded. This can be attributed to more uniform distribution of pressure over the sample surface. Even in cases where a particle or defect on the TJ2 sample surface was present, the unbonded area was significantly reduced compared with previous tests. The overall bonding yield improved significantly and this version of bonding procedure was used for fabrication of devices.

5.5 Summary

Wafer bonding is a key fabrication technology of the VCSEL design investigated in this project. Compared with other methods for hybrid integration, it gives necessary high material quality and can be CMOS-compatible and scalable. In this chapter two methods for wafer bonding are

discussed: the direct and adhesive wafer bonding. The basic mechanisms for bonding for both methods are shortly explained, and then specific implementations that can satisfy the requirements for this project are discussed.

In hydrophilic direct wafer bonding, molecular bonds are formed between polar –OH hydroxyl groups on the oxidized surfaces of the wafers when they are brought into intimate contact. During high-temperature annealing these strong covalent bonds are formed that permanently bond the two wafers. In order to achieve good bonding strength with direct bonding method without the use of high temperature annealing, samples are treated with oxygen plasma. This results in thin layer of oxide which is more hydrophilic. Followed by DI water treatment, high density of hydroxyl groups is formed on the surface. The strong covalent bonds can be formed by annealing the samples at much lower temperature, around 300 °C.

The direct wafer bonding has extremely strict requirement for ultimately flat and clean bonding surfaces. However, the III-V epitaxies that were obtained for this project had relatively rough surfaces with distinctive morphology and high defect density. Therefore, the direct wafer bonding method was not applicable and adhesive wafer bonding is implemented to reduce the surface requirements.

Adhesive wafer bonding relies on an intermediate layer of adhesive material to establish a bond between two wafers. The adhesive is applied in liquid form to planarize and fill any voids on the surfaces. Then the adhesive is hardened to establish the permanent bond. BCB polymer is the most popular adhesive used for wafer bonding. It is hardened by thermal curing at relatively low temperatures (250-300 °C), making it suitable for bonding of III-V and Si materials. The procedure for bonding with ultra-thin layers of BCB is discussed in detail and implemented.

Significant efforts and large number of tests were necessary to obtain stable bonding procedure with high yield even with roughest epitaxy. The change of available bonding tools resulted in major setbacks. Out of three different tools that were used during testing, the best results were obtained with NILT CPB balloon bonder, thanks to the uniform force distribution. This bonding procedure is employed for the fabrication of the hybrid VCSELs in this work, and will be summarized again in next chapter.

CHAPTER 6

Fabrication of hybrid VCSELs

6.1 Introduction

The aim of this work is experimental demonstration of proposed laser design. Fabrication of devices in cleanroom facility was the primary and most time-consuming task of this Ph.D. project. In this chapter, the fabrication of hybrid VCSELs will be presented starting with overview of fabrication process flow, followed by the details of most processing steps. Problems that were encountered and optimization steps that were undertaken will also be described.

6.1.1 CMOS compatibility

Silicon has been the main material for semiconductor electronics for the last 50 years. High-volume manufacturing using complementary metal-oxide-semiconductor (CMOS) processing of Si-based electronics has been continuously developed and perfected. Silicon-on-insulator (SOI) platform became popular as it offers reduced parasitic capacitance, for reduced operating voltage and greater operating speeds.

SOI platform also found application in silicon photonics. Transparency of Si in near infra-red wavelength range used in optical communications and the large refractive-index contrast with buried oxide (BOX) makes it ideal platform to build passive and active devices for guiding and manipulating light [222]. Use of CMOS processing means that Si photonic devices can be fabricated using mature fabrication infrastructure of silicon microelectronics, which enables low-cost high-volume production. State-of-the-art CMOS technology is sufficiently advanced to fabricate virtually all Si photonic components [20]. It enables dense integration of photonic devices and also opens door to integration of electronic and photonic components on the same chip.

Heterogeneous integration of III-V materials on SOI platform brings a new set of challenges to fabrication. If CMOS processing is used, any fabrication of hybrid devices needs to be carefully designed to be CMOS-compatible. In previous chapter, methods for wafer bonding that are CMOS-compatible have been discussed. Once the substrate is removed, the III-V processing of lasers can be done using standard fully CMOS-compatible processing.

6.2 Process flow overview

Complete process flow for fabrication of hybrid VCSELs will be described in short in this section. As the typical example, processing of v2 VCSEL version will be illustrated. Any significant differences for other versions will be noted.

Almost all of the fabrication during this project was done in state-of-the-art cleanroom facility at DTU Danchip, with the exception of proton implantation that was performed at the Ion Technology Center (ITC), Ångström Laboratory, Uppsala University.

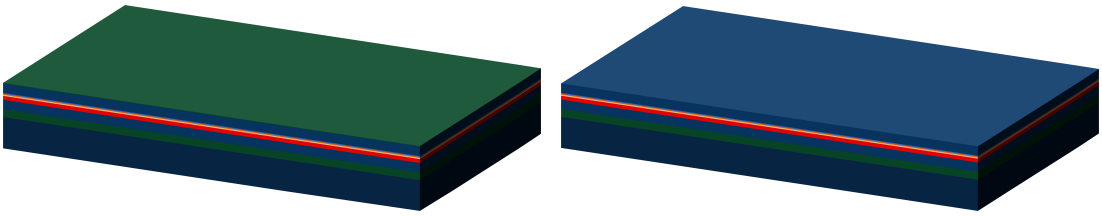
The fabrication step descriptions will be followed by schematic illustrations for most steps. These illustrations show a single device as it is fabricated. For the sake of understanding, the layer

thicknesses in the schematics are approximately on scale, apart from the InP and Si substrate that are shown only partially.

6.2.1 Sample preparation

Due to limited supply and high price of III-V epitaxial wafers, all fabrication is done on chip-scale. Both III-V and SOI wafers are covered with photoresist (PR) and cleaved into square dies. The photoresist acts as protective layer from particles and scratches during cleaving. Cleaving is done by making a small scratch near the edge of the wafer using a tungsten tip and then applying pressure on both sides of the scratch with tweezers. The bonding surface should not be directly scratched using the tip as the micro-sized scratches along the cleaved edges of the surface can cause bonding issue. Instead, the samples are scratched on the backside.

The III-V chip size is 7 mm × 7 mm, selected as a compromise between effort to save material, handling convenience and pattern of devices. The SOI chip size is 1.5 cm × 1.5 cm, chosen to fit the slot of the chip cassette for e-beam writer. Working with small samples instead of full wafers comes with some challenges. The spin-coating of materials on square samples results in thick edge beads that have to be removed since they can leave unwanted spacing between the sample and mask during lithography processes. Relative uniformity of deposited layers is also poorer due to smaller surface. Some of the tools in the cleanroom are not designed to handle small samples, so alternative tools, that are mostly not automated, need to be used. In some processes it is necessary to place the samples on a dummy carrier wafer so it could be processed in the tool.



(a) **(b)**

Figure 6.1: (a) Clean III-V sample. (b) Protective cap layer removed. Color legend: green – InGaAs, blue – InP, red – active region, orange – TJ, dark blue – InP substrate.

Cleaved samples are cleaned using with a solvent cleaning process to remove the protective PR and surface is inspected for any contamination or particles.

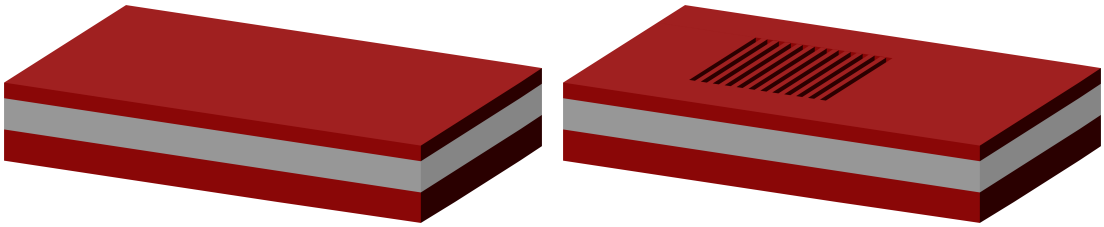
The III-V epitaxy has a protective cap layer (or pair of layers in case of pin epitaxy) grown last. By removing this layer, any contamination or particles would be lifted-off. The InGaAs cap layer is selectively removed by very short wet etching with 1 H_2SO_4 (96%) : 8 H_2O_2 (31%) : 8 H_2O. InP cap layer is selectively removed using 1 HCl (37%) : 4 H_3PO_4 (85%). This is illustrated on Fig. 6.1.

6.2.2 Fabrication steps

Patterning the SOI

First patterning step is done on SOI sample to define the HCG patterns, bottom alignment marks and bonding guides. Since the dimensions of the grating openings are sub-micron, standard UV photolithography cannot be used, and therefore e-beam lithography is necessary. All devices are arranged within 5 mm × 5 mm area that would be covered with III-V, and all alignment marks are positioned outside III-V area. Large guides for bonding, visible by eye, are used to place the III-V sample during bonding so that device area is completely covered.

The pattern is defined in the resist using e-beam lithography and then transferred into the Si layer of the SOI using dry etching. Fig. 6.2 illustrates SOI sample with grating pattern.

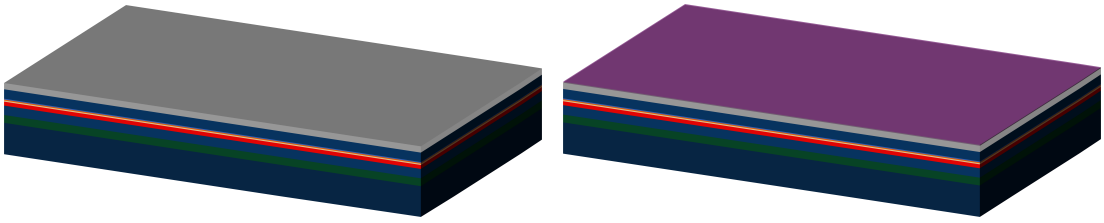


(a) (b)

Figure 6.2: SOI sample patterning before bonding. (a) Clean SOI sample. (b) Fabricated grating on Si layer. Color legend: Dark red – Si, grey – SiO_2.

Wafer bonding

The SOI sample is striped of resist and cleaned in heated RCA-1 solution (1 N_4OH (95–97%) : 1 H_2O_2 (31%) : 5 H_2O). On III-V sample, the dummy cavity layer is formed by depositing SiO_2 using plasma-enhanced chemical vapour deposition (PECVD) process. After that, diluted BCB (1:8) is spin-coated to act as a thin adhesive bonding layer (see Fig. 6.3). After short bake to evaporate the solvent and solidify the BCB, the sample is ready for bonding.

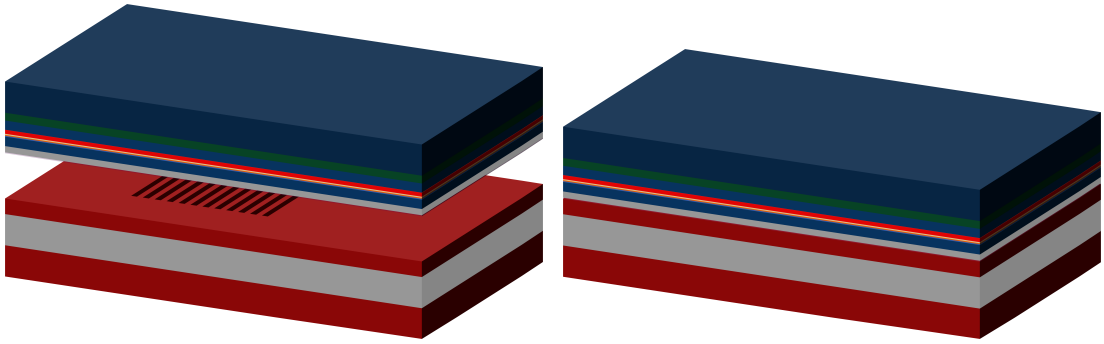


(a) (b)

Figure 6.3: III-V sample preparing for bonding. (a) Deposited dummy cavity SiO_2 layer. (b) Spin-coated thin BCB. Color legend: transparent purple – BCB.

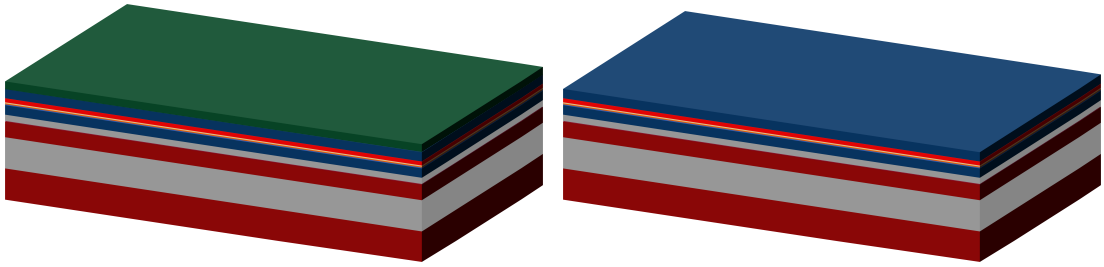
The prepared III-V sample is manually flipped and brought into contact with SOI sample, as illustrated on Fig. 6.4, and slight pressure is applied to stick two samples together enough so that III-V sample is not moved during transport to bonding tool. The mechanical bonding process is done at the temperature of 250 °C and pressure of 3–4 bar for 90 min. This process cures the BCB and permanently bonds the two samples together.

After bonding procedure is finished, the 350 μm thick InP substrate needs to be removed. This is done using wet etching process with HCl (37%). If the bonding process is done correctly, the bonding strength should be good enough so that wet etching would not cause debonding. The process takes approximately 1 hour, and stops when the InGaAs etch stop layer is reached, which is not etched by this etchant. The etch stop layer can also be selectively removed using 1 H_2SO_4 : 8 H_2O_2 : 8 H_2O wet etching, or it can be left to act as protective layer for following processes and removed later during fabrication. The bonded sample, after substrate and etch stop layer removal, is shown on Fig. 6.5.



(a) (b)

Figure 6.4: (a) III-V sample is flipped for bonding with SOI. (b) Two samples are bonded.



(a) (b)

Figure 6.5: (a) InP substrate is etched from the bonded sample. (b) InGaAs etch stop layer is removed.

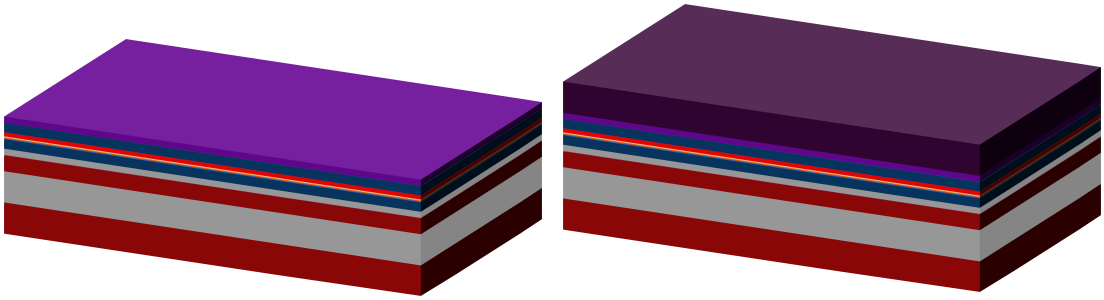
Mesa etching and implantation

The III-V epitaxy membrane bonded on SOI sample can now be processed to fabricate the devices. First step is to define individual devices by doing mesa etching. The laser mesas are aligned to cover the HCGs patterned on SOI. The etching of III-V epitaxy is done using plasma dry etching in RIE dedicated for III-V processes. This process requires hard mask, as the photoresist would be strongly affected by this type of plasma etching. Therefore, a 200 nm layer of silicon nitride (Si_3N_4) is deposited using PECVD process. Photoresist is spin-coated on nitride layer and patterned using standard UV lithography. The pattern is transferred from resist mask to nitride layer using dry etching in RIE with CHF_3/O_2 chemistry, and resist is removed using solvent. The hard mask creation process is illustrated on Figs. 6.6 and 6.7.

With such prepared hard mask, the III-V dry etching is done using cyclic metal organic reactive ion etching (MORIE) with $CH_4/H_2 - O_2$ chemistry. The Si_3N_4 has high selectivity (>10) to the III-V material for this kind of plasma etching, so the mask degradation is negligible. The etching is done all the way through the III-V epitaxy, until dummy cavity SiO_2 layer is reached, as illustrated on Fig. 6.8a.

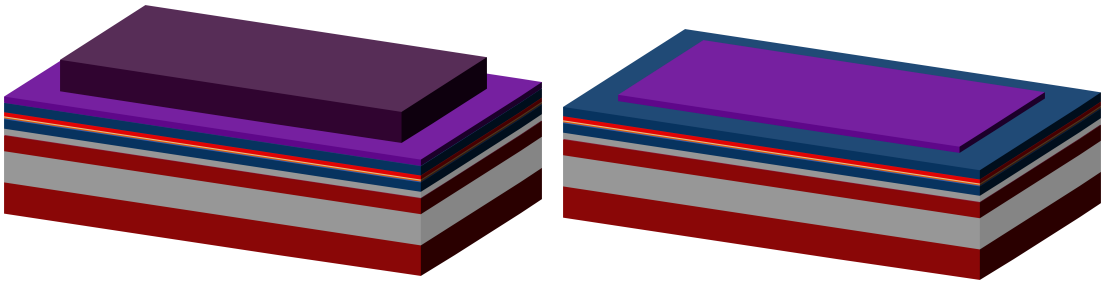
The hard mask is not removed at this point. It is reused for implantation process, for the versions which include implanted apertures. UV lithography is used again to create pattern for mask that would be used to protect the aperture and bottom contact area from implantation. After patterning the resist, dry etching is used to transfer the pattern to the existing Si_3N_4 layer. The resist is not removed. This mask pattern is depicted on Fig. 6.8b.

Proton implantation is next step. The ion energy is determined with simulations, as described in section 3.3. After implantation the resist is removed using solvent cleaning and O_2 plasma ashing. The remaining hard mask is removed using maskless dry etching.



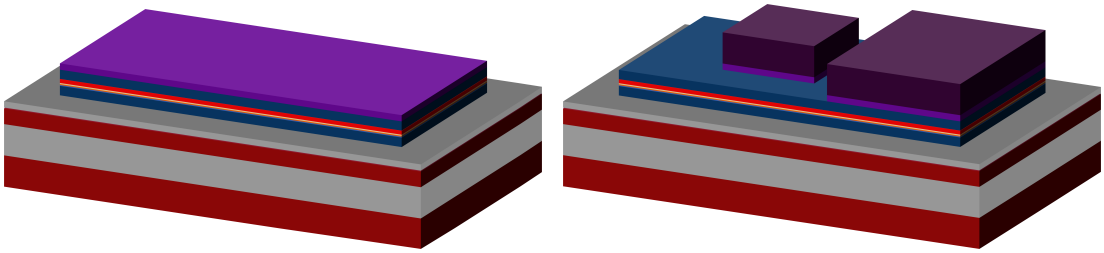
(a) (b)

Figure 6.6: (a) Si_3N_4 hard mask layer deposited. (b) Photoresist spin-coated on top of Si_3N_4. Color legend: magenta – Si_3N_4, dark purple – photoresist.



(a) (b)

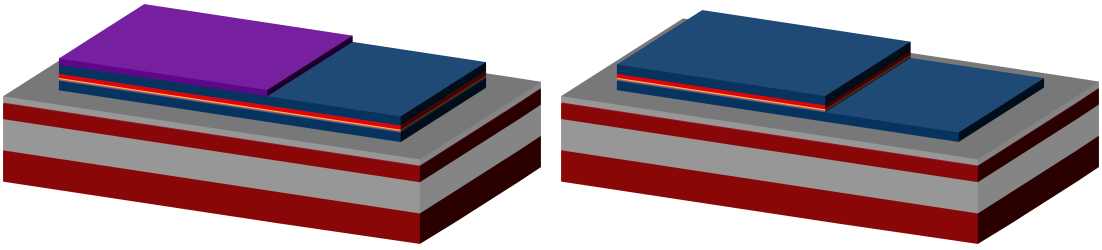
Figure 6.7: (a) Patterned photoresist mask. (b) Pattern transferred to Si_3N_4 using dry etching.



(a) (b)

Figure 6.8: (a) First III-V mesa formed by dry etching. (b) Mask fabricated for implantation.

Next task is to expose the bottom contact layer. This is done using partial mesa etch, where etching is stopped once the bottom contact layer is reached, as illustrated on Fig. 6.9. Hard mask is again fabricated. In case that implantation is not done, then Si_3N_4 layer of the first mesa hard mask can be patterned for second mesa mask. Otherwise, a new Si_3N_4 layer is deposited and patterned. The III-V etching is done as a combination of dry and wet etching. Dry etching is done until just bottom contact layer is reached. Short wet etching of InP contact layer is done to remove 20–30 nm of etched surface which would be damaged from ion bombardment. The hard mask is then removed.

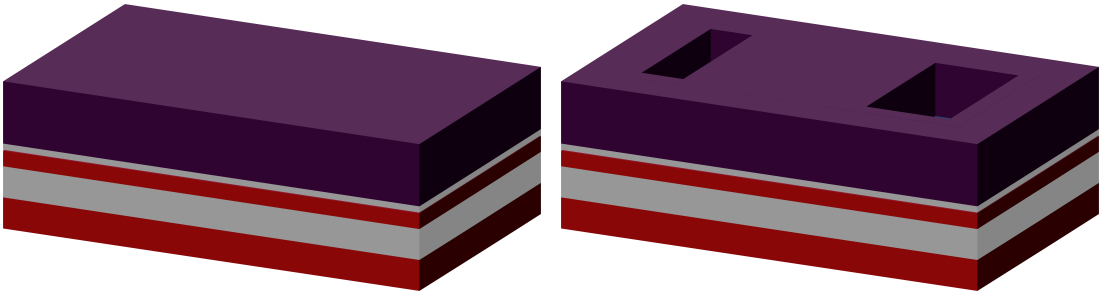


(a) (b)

Figure 6.9: (a) Hard mask for second mesa etching. (b) Second mesa etching is done to expose the bottom contact layer.

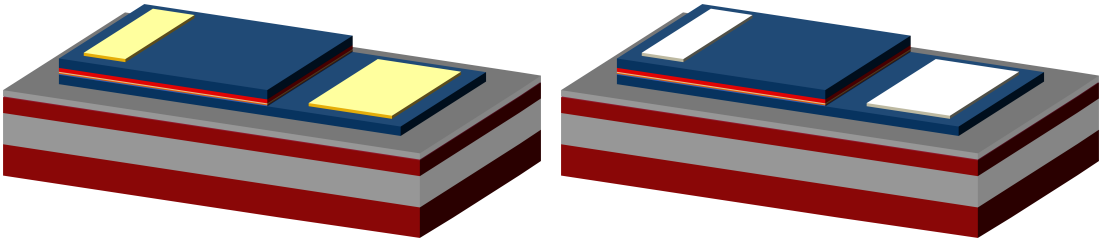
Formation of ohmic contacts

Ohmic contacts are fabricated next. Lift-off method is used to pattern the metal contacts. UV lithography with negative resist is done to create the mask with resist being removed only where contacts are to be deposited, as shown on Fig. 6.10.



(a) (b)

Figure 6.10: (a) Negative resist spin-coated over the sample. (b) Pattern for ohmic contacts defined in the resist.



(a) (b)

Figure 6.11: (a) Metal contacts after lift-off process, having golden color. (b) Ohmic contacts change color to silver after alloying.

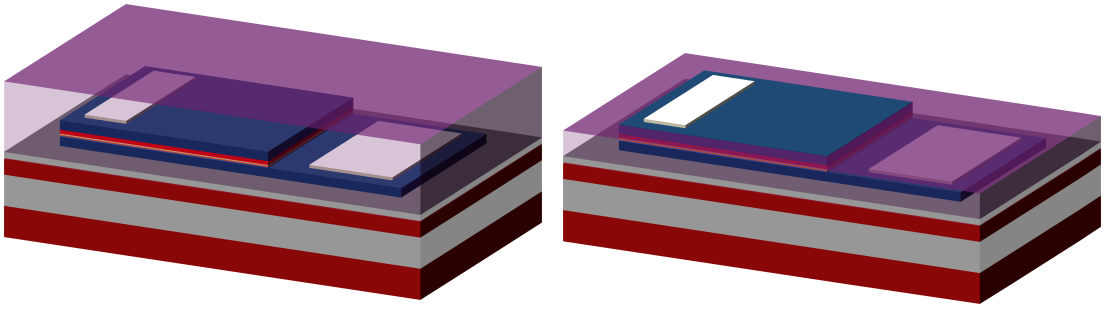
Metals are deposited using electron-beam evaporation. Two-step metallization is used, as described in section 3.4. At this step, the low-Au ohmic metal stack, consisting of 30 nm Ni, 50 nm Ge and 20 nm Au layers, is deposited. The sample is then submerged in solvent to dissolve the resist mask, which lifts off any metal that is deposited on the resist. Metal remains only in areas where openings in the mask were defined. RTA is used to anneal the contacts at around 420 °C

for 15 seconds. The annealed contacts change color from golden to silver-like, as is illustrated on Fig. 6.11. This thermal process also anneals the unwanted damages from implantation process. The isolation created in *p*-type layers should reach the maximum value around this temperature.

In case of V4 VCSELs with PIN epitaxy, *n*- and *p*-side contacts have to be fabricated separately. The *n*-type ohmic contact is again Ni/Ge/Au (30/50/100 nm) stack. The annealing is done for this contact, and then lift-off method is repeated again for top *p*-type contact with Ti/Pt/Au (30/50/100 nm) metallization. Alloying is not needed for this metallization to form ohmic contact.

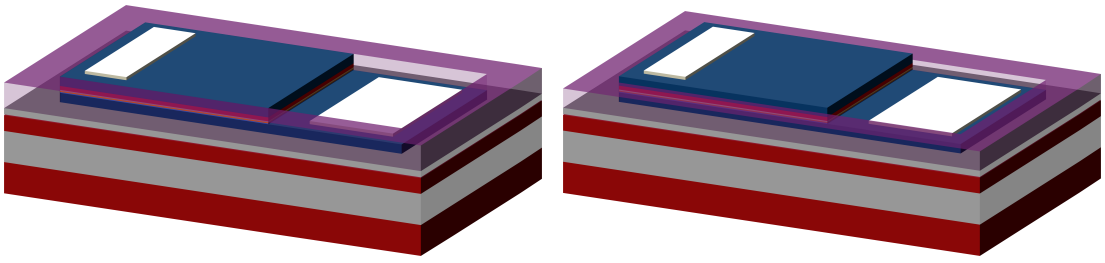
Planarization

Before the metal contact pads could be formed, the structure needs to be planarized. Thick layer of BCB is spin-coated over the sample and cured at 250 °C for about 1 hour. The BCB is then etched back using dry etching with O_2/CHF_3 RIE. The etch-back is stopped when the top of the mesa is exposed, as depicted on Fig. 6.12.



(a) **(b)**

Figure 6.12: (a) Sample planarized with thick layer of BCB. (b) BCB is etched back until top of the mesa is reached.



(a) **(b)**

Figure 6.13: (a) BCB covering the bottom contact is etched. (b) Height of the BCB layer is etched back to just above active region.

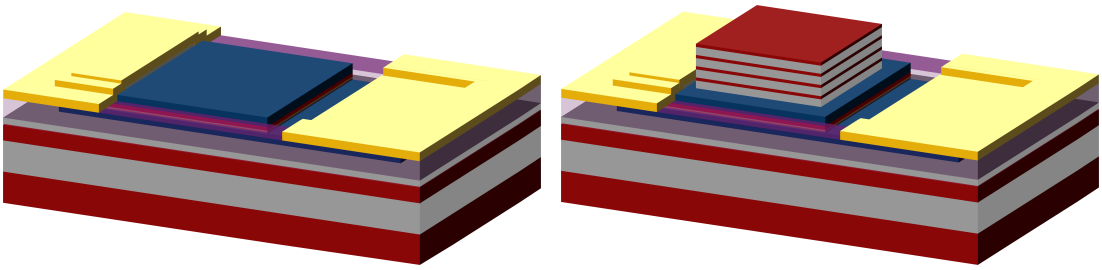
A resist mask is then defined to open the area of III-V mesa. The remaining BCB covering the bottom contact layer is then etched away (see Fig. 6.13). After removing the resist mask, the height of the BCB layer is reduced by doing maskless dry etch so that step height between bottom contact layer and BCB surface is reduced sufficiently to prevent disconnect of the deposited metal pads.

Formation of contact pads

The deposition of metals for contact pads represents the second step in two-step metallization scheme. The pads are designed to cover the formed ohmic contacts and extend over the planarized

BCB surface. In that way, they are electrically isolated from the substrate and from each other. The contact pad area is around 190 μm × 85 μm, designed to be more than sufficiently wide for placing the contact probes during characterization. Total footprint of a single device is 200 μm × 200 μm, with 50 μm spacing between nearby devices.

The lift-off method is again used to define the metal pattern. 10 nm Ti and 280 nm Au are deposited using e-beam evaporation. The Au layer thickness is sufficient to prevent disconnects at the steps between the BCB and ohmic contacts. The illustration of the structure with formed contact pads is shown on Fig. 6.14a.



(a) **(b)**

Figure 6.14: (a) Contact pads are formed. The area of the pads expands over greater area that is not shown on this illustration. (b) DBR mirror is formed on top of the mesa to finalize the device.

Dielectric DBR fabrication

Final part of laser fabrication is the top mirror which is formed as dielectric DBR. Three to four pairs of $\lambda/4$ layers of silicon dioxide (SiO_2) and amorphous silicon (a-Si) are deposited using PECVD. The a-Si deposited using PECVD has high refractive index around 3.67. The layer thickness is adjusted for each version and targeted wavelength.

The DBR is patterned using dry etching. Standard UV lithography is used to create the resist mask for DBR mesas in areas where laser resonator is to be formed, aligned with HCG underneath. Dry etching is done using RIE with CHF_3/O2 plasma optimized for etching SiO_2. The resist needs to be thick to survive the hour long etching process, so the thickness is around 2.3 μm. After removing the resist, the device fabrication is finished. Schematic illustration of completed device is shown on Fig. 6.14b.

6.2.3 Summary and remarks

Full fabrication process flow is briefly given and illustrated in this section. It consists of:

- wafer bonding of chips;
- one e-beam and six UV lithography steps processes;
- multiple depositions of dielectrics
- dry etching of Si, III-V, dielectrics and BCB;
- wet etching of III-V materials;
- ion implantation;
- two separate metallizations and lift-offs;
- planarization with BCB.

As can be seen, a broad range of fabrication processes are needed to make the lasers. The processing starts with bottom mirror (HCG defined on SOI) and ends with top mirror (dielectric DBR fabrication). The sequence of the processing steps is carefully considered: the SOI needs to be processed before bonding; the implantation has to be done before ohmic contacts are formed as the contacts would mask the area that should be implanted; the contact pads are formed before the DBR process, since the DBR etching would affect the BCB and change its height.

The extensive characterization follows most of the processes during fabrication. This was not mentioned in the process flow overview for simplicity. The thickness of deposited layers is measured using ellipsometry tools, and profilometer is used to measure the heights of different structures. The optical microscope is used to monitor the fabrication visually and verify the alignment and developing after each lithography step. SEM is used to take a closer look at the sample when optical microscope is not sufficient. Dry etching is controlled using in situ interferometer. The parameters and recipes for processes are continuously updated and adjusted with regards to results of previous fabrication steps. Many steps require testing and calibration before the process is done on the laser sample.

Total fabrication of one sample takes one to two months to complete. This long cycle time is a consequence of several factors besides the process flow complexity. Chip-scale processing limits the possibility of automatization and requires manual handling at many steps. Tight margins for alignment, that are imposed by design, mean that alignment of each lithography mask needs to be done carefully, verified and even repeated if misalignment is too large. The conditions and recipes for many processes do not hold over time, as the processing tools are used by different users for different processes. Therefore, calibration and testing before many steps drastically affects the total fabrication time.

In appendix A the process flow steps are listed in more details and parameters of processes. The parameters are given as used in tools available at DTU Danchip during the duration of this project, and results could vary over time or if process is implemented in different machine. In the following sections, individual processing steps will be discussed in more detail.

6.3 Patterning the SOI

After preparing and cleaning the samples, the fabrication of hybrid VCSELs starts with patterning the SOI sample. This consists of two main steps: lithography to define the pattern and dry etching to transfer the pattern on the top Si layer of the SOI. Some of the challenges and optimization of these two process will be described in this section.

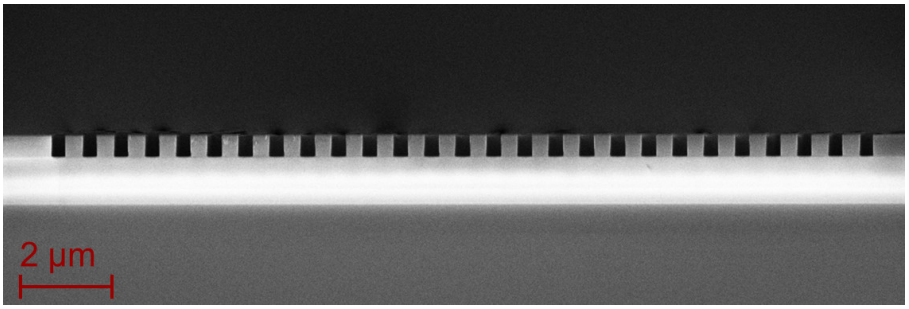


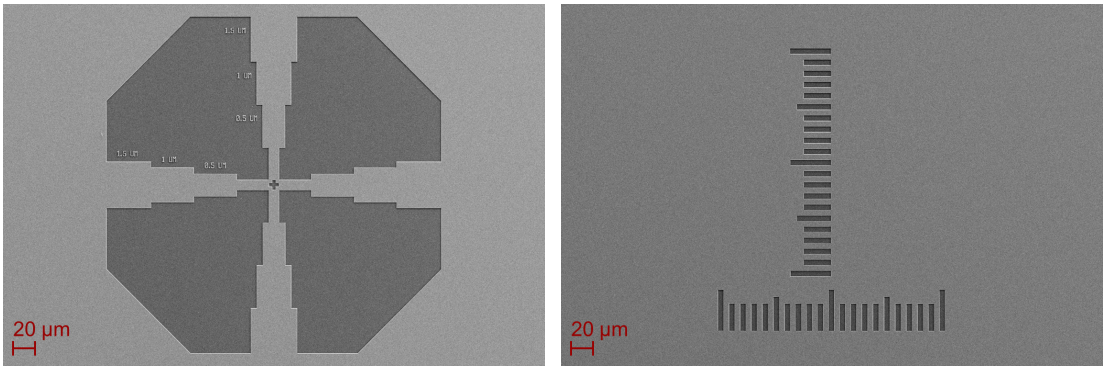
Figure 6.15: SEM image of cross-section of a grating fabricated on SOI sample. The grating is etched into the Si device layer of the SOI.

6.3.1 Pattern

The main and most critical part of the pattern is the array of gratings. 21×20 gratings are arranged in a grid within 5 mm $\times$ 5 mm area. This area will be covered with III-V sample after bonding. To help position the III-V sample, large guides that would be visible by eye are defined also. Outside this area all alignment marks that will be used for alignment in following lithography steps are placed, as well as the development-check marks.

The grating size is defined by the targeted mode size. Devices with mode sizes of 5, 7, 9, 11 and 13 μm are designed. The size of the heterograting well is designed to match those dimensions. The grating parameters for each version of VCSELs are given in chapter 4. However, to anticipate

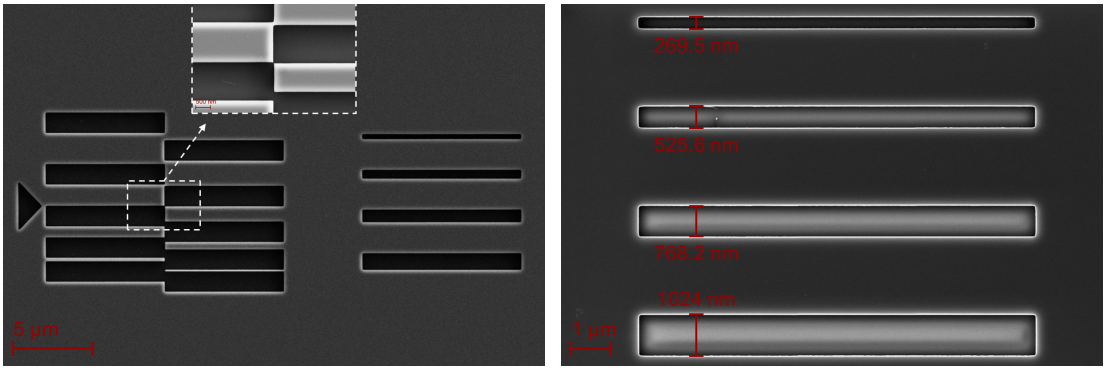
possible fabrication tolerances and uncertainties which could shift the resonance wavelength of the lasers, four variations of grating duty cycle (DC) are used over the sample. DC is varied so that resulting grating bar width is offseted from -5 to +10 nm, with increments of 5 nm. Designs with different variations of size and DC are distributed across the sample, so that uniformity of the device performance could be estimated, and in case some area doesn't survive fabrication the same device could be found on other surviving parts of the sample.



(a) **(b)**

Figure 6.16: SEM images of alignment marks defined on SOI that will be used for alignment in following lithography steps. (a) Female alignment mark, (b) bottom Vernier scale.

Two types of alignment marks are used: cross marks and Vernier scales. The cross marks are designed as "male/female" structures, but with four segments with separation widths between male and female mark 0, 0.5, 1 and 1.5 μm. The Vernier scales are designed with 5 μm wide rectangles that are separated by 5.25 μm on bottom pattern and 5 μm on top pattern. Therefore, the Vernier scales offer resolution below 0.25 μm. The Fig. 6.16 shows SEM images of bottom patterns of these two types of alignment marks etched into SOI. Their use and augment precision issue will be discussed more in section 6.5.



(a) **(b)**

Figure 6.17: (a) SEM image of structures used for estimating e-beam lithography pattern transfer. Inset gives closer look at the center of the structure. (b) Test structure for measuring the pattern offset. Lines are designed with widths of 250, 500, 750 and 1000 nm. Offset of 20-25 nm is observed.

The development-check marks are designed to verify the lithography process, mainly the resist development after exposure. These structures can be quickly checked using optical microscope to verify the development process. SEM can be used to further characterize the pattern, however it

will expose the resist. Their design is shown on Fig. 6.17a. The array of 1.25 μm wide rectangles are designed with varying spacing and offsets. The triangle points to a line at which a pair of rectangles should be perfectly aligned at corners. The inset shows a closer look of the alignment point. In case of overdevelopment, the thin separations between structures would disappear, and alignment point would shift to upper pair of rectangles. The second part of the development-check structure is used for direct measurement of the width offset after etching. Rectangles with widths varying from 250 to 1000 nm are designed. In the example shown on Fig. 6.17b, the rectangles have 20–25 nm larger width. This information was used for adjusting the grating design.

6.3.2 E-beam lithography

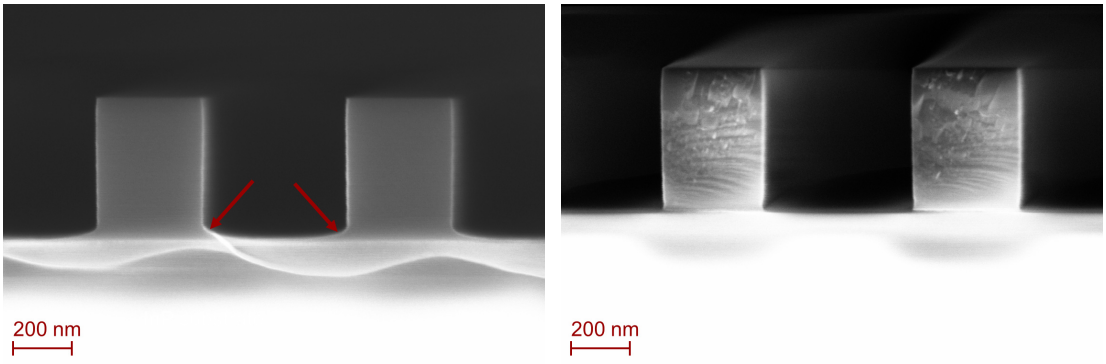
Since the dimensions in grating pattern are sub-micron and very high precision is necessary, patterning cannot be done using standard UV lithography. Deep UV (DUV) could potentially provide sufficient resolution, but the DUV stepper available in DTU Danchip is not available for chip size samples. Therefore, e-beam lithography is used.

High-resolution positive-tone e-beam resist ZEP520A (ZEON Chemicals) is diluted with Anisole in 1:1 ration so that concentration is 5.5%. It is spin-coated onto the SOI sample using manual spin-coater for 60 s at speed of 3000 rpm, and baked on hotplate at 160 °C for 2 min. The resulting resist thickness is around 145 nm. The exposure is done using JEOL JBX-9500FS electron-beam writer with acceleration voltage of 100 keV at DTU Danchip. The exposure parameters have been previously optimized in our group. The exposure dose of 250 μC/cm^2 with 2 nA current has been used for optimum results. After exposure, the pattern is developed using ZED-N50 (ZEON Chemicals) developer for 60 s with slight agitation by hand. Postbake process is done at 100 °C for 3 min to harden the resist, which then works as a hard mask.

6.3.3 Si dry etching

Surface Technology Systems (STS) advanced silicon etcher (ASE) is used to transfer the pattern from resist mask to top Si layer of SOI sample. It is a deep reactive-ion etching (DRIE) method that uses C_4F_8/SF_6 chemistry for etching. In order to ensure excellent anisotropy, the Bosch process is implemented. The etching is done in cycles, where every cycle contains etching and passivation step. The etching step last 5 s after which passivation layer is deposited using C_4F_8 gas source for 3 s. The passivation layer protects against the further chemical attack, but it is removed from the bottom of the trenches due to directional bombardment with ions during etching step. Therefore, the sidewalls remain protected while etching continues at the bottom. The etching depth is controlled by setting the number of cycles. Smooth vertical sidewalls are desirable as any roughness would lead to scattering of light and angled profile would affect the grating properties.

Testing has been done to investigate the quality of the etch, sidewall profile and determine the number of cycles required for etching through the 480 nm thick Si layer of the SOI. Test samples are prepared with grating pattern, etched using ASE with varying number of cycles and then cleaved so that grating profile could be examined. The Fig. 6.18 shows SEM images of the cross-section of grating structure after 11 and 12 cycles of etching. The sidewall profile looks smooth and no angle is noticeable. The 11 cycles seem to not be enough as the bottom of the trench has bowl-like shape, and some remaining Si is noticeable at the foot of the grating bars, as marked with red arrows on Fig. 6.18a. This could degrade the performance of the HCG. With 12 cycles all of the Si seems to be removed from the bottom of the trench and SiO_2 BOX layer is reached. 13 cycles resulted in undercutting at the foot of the grating bars. Therefore, the 12 cycles are used for laser fabrication. The measurement of resist thickness after etching with 12 cycles shows about 60 nm left, so the resist thickness is enough to maintain good pattern. The resist can then be stripped using Microposit™ Remover 1165 (DOW Electronic Materials).



(a) (b)

Figure 6.18: SEM image of cross-section of a grating bars etched into SOI using ASE Bosch process with (a) 11 cycles and (b) 12 cycles. The red arrows point at remaining Si due to unfinished etch with 11 cycles.

6.3.4 Grating bar width control

Parameters of the HCG need to be well controlled within accepted tolerance. Larger deviation can lead to shift of the resonance wavelength of the cavity and VCSELs might not be able to lase. The challenge comes from the inevitable deviation from design during lithography and etching processes, as illustrated before on Fig. 6.17.

There are two approaches in solving this challenge: (a) the lithography and etching processes can be further optimized to get result that matches the design or (b) the deviation can be characterized for a fixed process and then compensated by changing the design. The approach (a) could take significantly more time and may never reach the perfect result. Therefore, the approach (b) was chosen. The downside of (b) approach is that it is only reliable as long as processes are not changed and give repeatable results.

The grating period is always almost perfectly reproduced from design, with no effect by changes in exposure, development or etching. The only way period can be disturbed is if the grating falls on the border of the stitching field of the e-beam writer. Then, deviations as much as 20 nm are possible. Therefore, the stitching fields are set up in a way that no grating sits on the border.

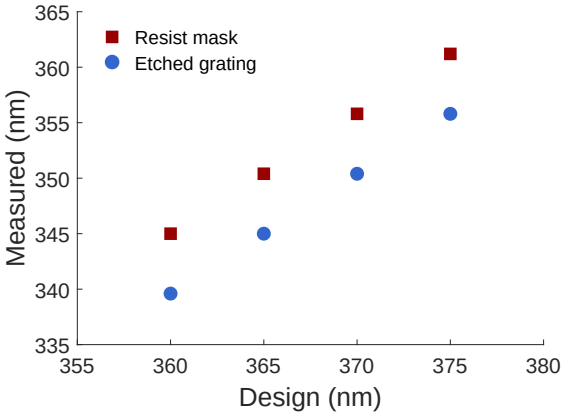
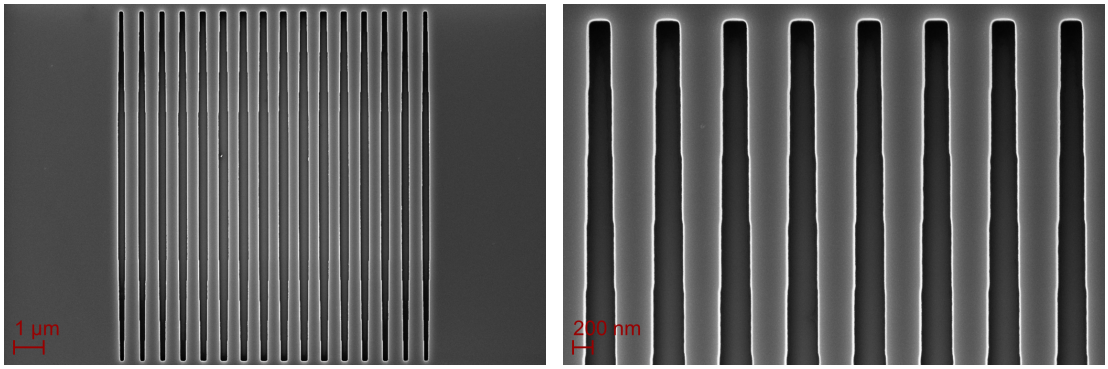


Figure 6.19: Measured width of the grating bar versus designed width. Measurement of resist mask and resulting etched Si grating$_p$ are done using SEM.

The openings in the resist, however, can have significant deviation. From the results shown previously in Fig. 6.17b, suggest that deviation can be in range of 20–25 nm over the range of 250

to 1000 nm wide openings. The test was done to determine more precisely the deviation around the targeted grating bar width. Four different gratings are designed with offsets of 15, 20, 25 and 30 nm added to targeted grating bar width. The bar widths are measured using SEM on mask before etching and on resulting etched pattern after resist is removed. The results are plotted on Fig. 6.19. The deviation on the mask patter were around 15 nm, while the etched pattern showed deviation around 20 nm. Therefore, for targeted 345 nm grating bar width, the design should be 365 nm. The 5 nm difference between mask and etched pattern is taken into account when grating pattern is characterized during full laser fabrication. As mentioned before, other deviations, fabrication tolerances and uncertainties during rest of the processing could shift the resonance wavelength of the lasers. To account for that possibility, designs with varying HCG bar width are designed on each sample. So, additional offset of -5 to +10 nm is added to determined 20 nm for different gratings.

The grating bar width is also varied to create barriers of the heterograting for optical mode confinement. The grating parameters are slightly changed every Λ distance from the well. For example, in case of v1 the bar width was reduced by 10 nm, while in case of v2 it was increased by 4 nm. The desired change was always observed during characterization, within the resolution of the SEM. An example of heterograting with exaggerated barriers is shown on Fig. 6.20. The grating bar width is increased by 20 nm at every step.



(a) **(b)**

Figure 6.20: SEM image of a heterograting with exaggerated barriers. (a) Grating overview. (b) Closer look at barrier transitions. The grating bar width is increased by 20 nm every Λ length.

6.4 Bonding of samples and III-V substrate removal

Wafer bonding methods are discussed in detail in chapter 5. The adhesive bonding using ultra-thin BCB polymer has been implemented and optimized. In this section, the process will be summarized and specific details will be given.

6.4.1 Preparation for bonding

The first step in preparation for bonding process is rigorous cleaning of the sample. The III-V sample is cleaned by selective wet etching of protective cap layers as discussed before. The patterning of the SOI sample was done before bonding, and resist was removed using solvent. However, as shown on Fig. 6.21, the residuals of the resist always remain after resist stripping. This contamination can be removed using O_2 plasma ashing. However, RCA-1 cleaning is also sufficient.

The RCA-1 solution is prepared by mixing H_2O and NH_4OH and heating it up until 70–80 °C. Then H_2O_2 is added and temperature is stabilized before the SOI sample is dipped and kept in

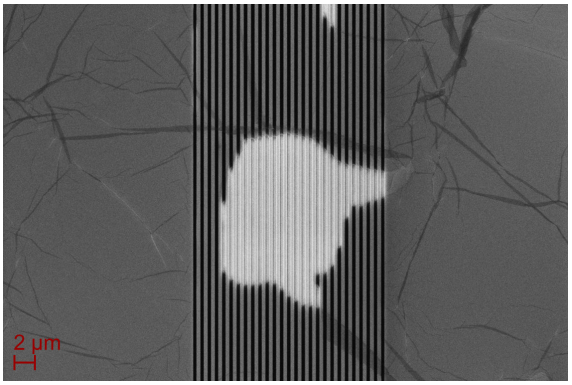


Figure 6.21: SEM image of a test grating structure on SOI after e-beam resist removal with 1165 solvent. Bright stains and dark string-like residuals of resist are visible.

for 10 min. Bubbles can be seen originating from the surface of the sample where the solution is reacting with contamination. The sample is then carefully rinsed with running DI water and blow dried with N_2 gun.

Next, the dummy cavity layer is formed by depositing SiO_2 using low RF-frequency (380 kHz) PECVD process. A small clean Si sample is placed together with III-V for the process, and oxide thickness and refractive index is measured using ellipsometry on dummy Si sample. Test are done beforehand to calibrate the exact process time for desired thickness, as the chamber conditions change over time.

The III-V sample with oxide layer is spin-coated with Cyclotene 3022-35, diluted with mesitylene to 1:8 ratio by volume, using manual spin-coater for 40 s at 3000 rpm. Due to small size of the sample, BCB usually contaminates the back side of the sample which needs to be carefully cleaned using mesitylene. The sample is baked for 1 min at 160 °C to evaporate the mesitylene and reflow the BCB layer.

6.4.2 Manual and mechanical bonding

The prepared III-V sample is manually flipped, so that BCB covered side faces down, and placed on top of the SOI sample. Tools for precise placement can be used, however it is not necessary in this case. Bonding guides have been designed and etched into the SOI, and they provide visual guidance where III-V sample should be placed to cover the area with gratings. Slight pressure is applied to the III-V sample from the center, to ensure good contact. The samples are not strongly connected at this point, so careful handling is necessary not to disturb the samples before mechanical bonding.

The sample stack is loaded into the "balloon" type bonder, NILT CPB. The plot of the temperature and pressure are illustrated on Fig. 6.22. The temperature is risen to 150 °/min with 10 °C/min ramp. The pressure of 4 bar is applied and temperature is kept for 10 min at 150 °C for precuring of BCB. The BCB is at its softest state and under applied pressure it is reflowing and adapting to any surface morphology. Then temperature is slowly risen with 2 °C/min ramp to 250 °C, where BCB is hard cured for 1.5 h. Finally, samples are cooled down to 50 °C, when the chamber is pressurized and they can be unloaded.

6.4.3 InP substrate wet etch

After bonding procedure is finished, the 350 μm thick InP substrate needs to be removed. This is done using wet etching using wet etching only or with combination of grinding and wet etching.

Grinding the substrate can be done using lapping tool and a slurry made from a suspension of aluminum oxide abrasive powder with 3 μm particle size. By grinding the substrate most of the way,

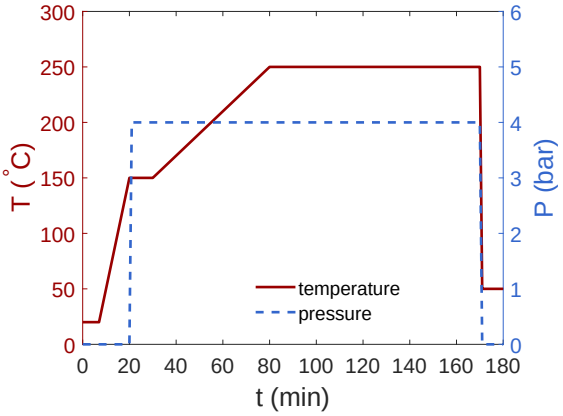


Figure 6.22: Plot of temperature and pressure versus time in bonding recipe.

and then finishing with wet etching, the time that sample spends immersed in aggressive etchant can be reduced. This method was used in some of the testing. However, on several occasions, it led to cracking of the sample due to difficult handling of the tool and small sample size. Therefore, in most of the cases substrate was removed using only wet etching.

Wet etching of InP is done using aqueous solution of HCl (37%). This is the critical step that shows the quality of the bonding. Even though the BCB doesn't provide hermetic seal, the bonded interface of III-V is protected from etching by the SiO_2 layer. The process usually takes approximately 1 hour, and stops when the InGaAs etch stop layer is reached, which is not etched by this etchant. However, the HCl etching of InP is anisotropic and it doesn't etch the exposed (01-1) planes [220, 223]. This results in large unetched ridges of InP on the two opposite edges of the bonded epitaxy. The Fig. 6.23a shows a photograph of one example of a bonded sample before the InP substrate is removed, and photograph of the same sample after substrate is removed using wet etching is shown on Fig. 6.23b. The unetched ridges are visible on two opposite edges of the sample. The slopes of the ridges are (211)A crystallographic planes with angle of $\sim 35\,^\circ$ relative to the (100) plane of the flat surface. These ridges can be several hundreds of micrometers high. They would prevent intimate contact between the sample and photolithography masks, which would deteriorate the lithography resolution. Therefore, the ridges need to be removed before the processing can be continued. This can be done using one of several isotropic wet etching solutions for InP [220, 223], however considering that they lie outside the region where devices will be patterned, the ridges were simply carefully cleaved off using sharp tungsten tip. Photoresist layer is first spin-coated on the sample to protect the surface from particles that are generated during cleaving. The photograph of the sample after removal of ridges is shown on Fig. 6.23c

The InGaAs etch stop layer can now be selectively removed using 1 H_2SO_4 : 8 H_2O_2 : 8 H_2O wet etching. However, in most cases it is left to act as protective layer to avoid surface damage of the contact layer during hard mask deposition and plasma ashing steps in following processes. It is then removed after mesa etching is finished and before the ohmic contacts are formed. The exception to this is v4 version with PIN epitaxy. Since the top contact layer is InGaAs, a pair of InGaAs/InP etch stop layers are used. It would be too complicated to remove them selectively after the mesa etching is done, so they are removed Imediately after substrate removal.

6.5 UV Lithography and alignment

Following processing of bonded III-V epitaxy is based on standard UV contact lithography. Pattern on the photolithography mask is aligned to the marks previously defined on the SOI by e-beam lithography, so that devices are fabricated exactly on top of the gratings. Overall process of photolithography process will be described in this section. The issues with resolution, pattern quality and alignment will be discussed and test structures will be explained.

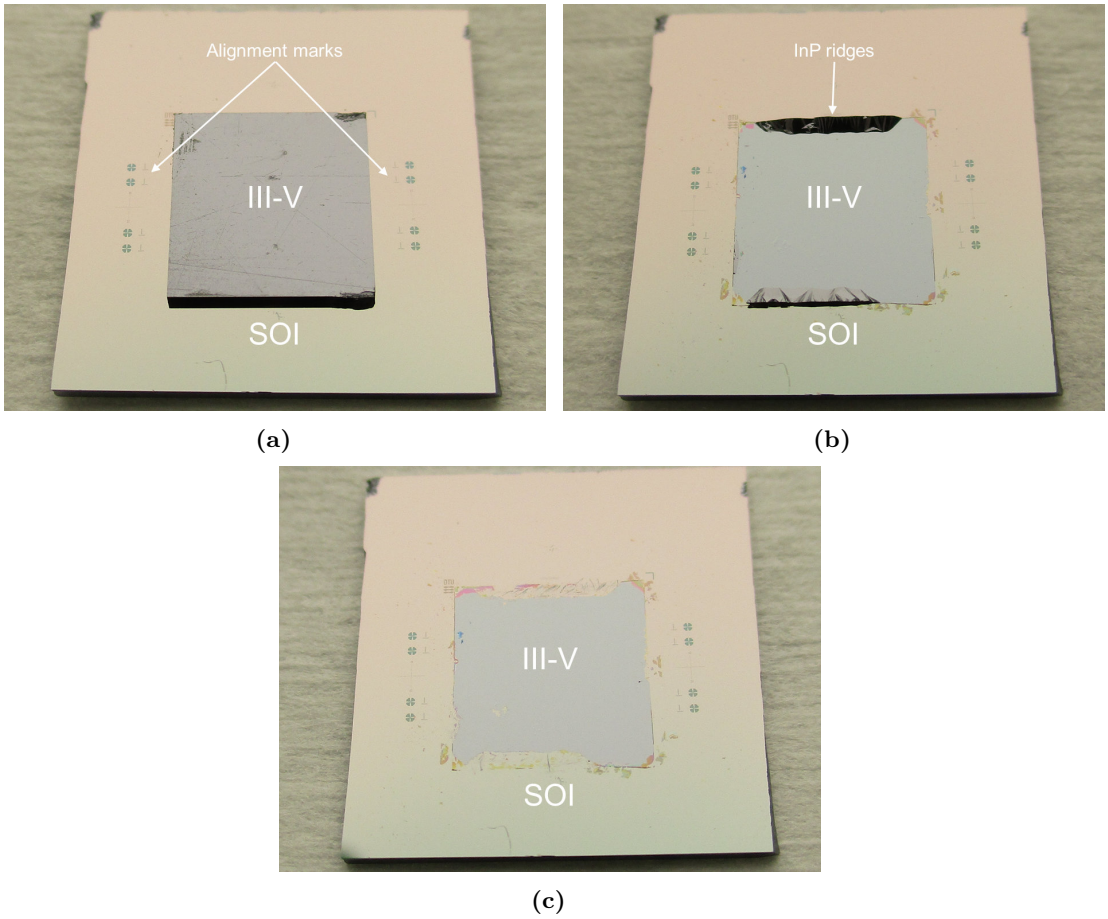


Figure 6.23: (a) Photograph of the bonded III-V and SOI samples before substrate removal. The sets of alignment marks are visible on both sides outside of III-V area. (b) The same bonded sample after substrate removal. Large InP ridges are visible on two edges of the sample. (c) The bonded sample after the ridges have been cleaved off.

6.5.1 Overview of photolithography processes

In general the photolithography process consists of five steps:

- surface pretreatment for adhesion;
- photoresist application;
- softbake;
- UV exposure thorugh the mask;
- postbake;
- development.

Surface pretreatment is often necessary as photoresists are usually hydrophobic and have very bad wetting with hydrophilic surfaces such as dielectrics or native oxides. Vapor priming with hexamethyldisilazane (HMDS) before the spin-coating is used to promote the adhesion for photoresist. The priming process is done in a dedicated oven which prebakes the sample at 150 °C for 5 min, followed by HMDS priming for another 5 min. The process dehydrates the substrate surface, and converts the surface into hydrophobic with lower surface tension. During experiments, without the adhesion promoter smallest features of the pattern would commonly not remain after development.

The photoresist is applied to primed surface by spin-coating. Due to the small sample size,

manual spin-coating tools are used, as the automated spin-coaters are designed to handle wafers only. The resist is dispensed manually on the surface of the sample, which is then spanned with preprogramed speed, acceleration and time. The spin program usually consists of two steps: a 5 s spin at low speed of 500 rpm is done first to spread out the dispensed resist over the sample, followed by a determined high-speed spin to reduce the thickness to desired level. The choice of photoresist depends on the targeted polarity of the mask. Both positive and negative photolithography is used during laser fabrication. AZ 5214E (MicroChemicals GmbH) photoresist is used for positive tone lithography, and AZ nLOF 2020 (MicroChemicals GmbH) photoresist is used as negative photoresist for lift-off processes.

The exposure is done in Süss MicroTek Mask Aligner MA6 with 365 nm wavelength (i-line). It offers vacuum, hard, soft and proximity contact exposure. Vacuum contact offers the best pattern transfer. However, due to a technical flaw of the mask holder, during the vacuum process the mask would be shifted slightly, causing random misalignment at the order of micrometer. For that reason, hard contact was used until the flaw was fixed. The exposure dose is optimized for accurate pattern transfer for each type of photoresist and its thickness. Details with exposure intensity and dose for all the steps are listed in appendix A.

Post exposure baking is necessary only for negative tone lithography to ensure cross-linking of the exposed resist.

The development of AZ 5214E positive photoresist is done using a spray-puddle developer tool. It uses the TMAH-based AZ 726 MIF developer (MicroChemicals GmbH). Development time is usually 60 s. The pattern on negative AZ nLOF 2020 is developed manually in a beaker using same developer, due to more drastic sensitivity to development time.

Finally, another baking step can be optionally done. This can help harden the resist more to increase its resistance to etching, however it also causes the reflow of the resist which can affect the pattern. In most cases it was not found necessary.

6.5.2 Pattern quality and resolution

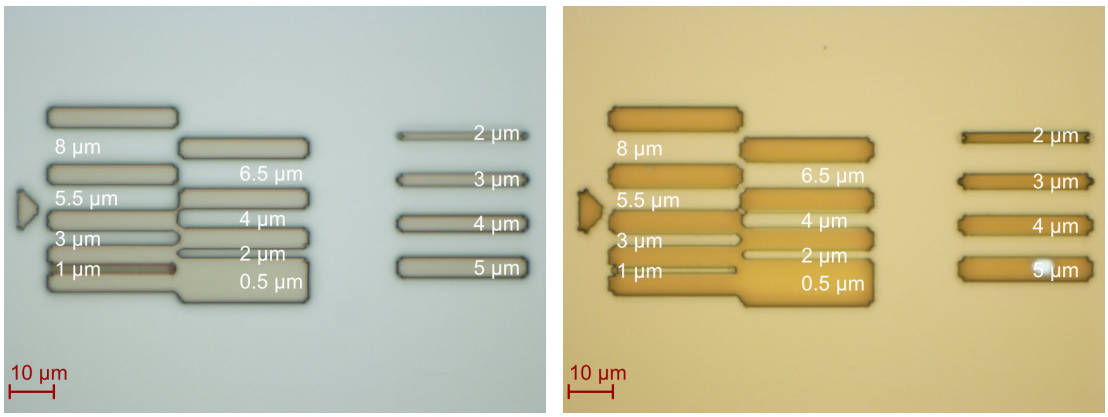
When different designs of the VCSELs have been described in chapter 4, it was mentioned that device dimensions are minimized with very narrow spacing between different parts of the structure. The tolerances are below 1–2 μm. Misalignment or development issues can lead to degraded optical or electrical properties of the structure. Therefore, it was necessary to control the photolithography process carefully.

Every step of the lithography process described previously can affect the resolution. However, the exposure and development processes have been identified to have the most precise influence. For positive photoresist process the optimization was focused mostly on exposure. The optimum exposure dose and development time were easily optimized, however the critical issue was the contact between the sample and the mask. For clean and flat test samples, with vacuum contact exposure excellent pattern transfer was obtained, with features as small as 1 μm and proper corner and edge definition. However, in case of the laser sample, different structures already fabricated can cause the varying separation between sample and mask. Any leftover protrusions from InP ridges that result from substrate removal process, can cause several micrometers of separation. Previously mentioned issue with alignment when vacuum contact mode is used forced the use of hard contact mode. The edge beads result from spin-coating of resist, and if they are not removed they too will create the spacing between the mask and sample. All of this leads to slightly poorer resolution and appearance of defects such as rough edges or "mouse-bitten" corners.

Negative tone photolithography was more difficult to control. The results would vary over time significantly. Apart from varying pattern transfer quality, the exposed part of the resist would often not get sufficiently resistive to developer, so resulting pattern would be overdeveloped and mask thickness would be reduced with no negative slope of sidewalls. This then made lift-off process unreliable. Therefore, the process was tested and optimized for every laser fabrication. The development process was done manually in a beaker, so that exact development time could be controlled. The pattern is regularly verified using optical microscope and additional developing is

done until satisfying result is achieved. It was eventually discovered that unreliable behavior was caused by the fact that resist was often past its expiry date.

For verifying the quality of the pattern transfer test structures are designed, similar to those used for e-beam lithography shown on Fig. 6.17. These "development-check" marks consist of two parts: (1) an array of rectangles, arranged with varying spacing between them from 0.5 to 8 μm; (2) an array of rectangles with varying width from 2 to 5 μm. The first part can be used to determine the resolution by observing the smallest opening between two structures. The second part can be used for measuring the offset of dimensions of individual structures and judging the smallest possible structure. Fig. 6.24, shows an example of such marks for positive and negative tone resist. It can be seen that spacing in the range of 0.5 μm could not be defined, and two structures are joined. 1 μm features are at the resolution limit, with some residual resist visible in the spacing between two rectangles for positive resist. For negative resist the mask openings are slightly wider than designed, in range of 0.5–1 μm as the corresponding 1 μm spacing is still defined.



(a) **(b)**

Figure 6.24: Microscope images of development-check marks for (a) positive and (b) negative tone resist. On Fig. (a) the structures are the resist mask, while on Fig. (b) the structures are the openings in the resist.

6.5.3 Alignment marks and precision

For fabrication of one VCSEL sample, six photolithography steps are used. All masks are aligned to the alignment marks that are defined precisely on the SOI sample using e-beam lithography. With so many lithographies, the misalignments add up with each subsequent step and could lead to fabrication issues. Therefore, it is crucial for alignment at every step to be as precise as possible, well below the design tolerance of 1 μm. The limit to manual alignment precision is the magnification power of the microscope of the aligner tool. The maximum magnification that was available was 10x. At this level, the 1 μm features are barely noticeable. The separation between the mask and the sample during alignment process is necessary, but it results in different focus and blurring of edges of one of the marks.

Two types of alignment marks are designed: cross marks and Vernier scales. The cross marks are designed as "male/female" cross structures, but with four segments with increasing separation widths between male and female mark of 0, 0.5, 1 and 1.5 μm on both sides. If the patterns are misaligned by 0.5 μm in one direction, the spacing on one side of second segment will disappear while on the other side it will increase to 1 μm and become visible. The Vernier scales are excellent visual aid to increase the resolution of the measurement. It contains two scales with different separation between graduations, and the central graduation marks on two scales are designed to be co-incident if alignment is perfect. By observing which of the top scale graduations is co-incident with a graduation on the bottom scale, misalignment can be judged. This is easier to perceive

by eye compared to estimation of spacing between two marks of the cross marks. The scales are designed with 5 μm wide rectangles that are separated by 5.25 μm on bottom pattern and 5 μm on top pattern. Therefore, the Vernier scales offer resolution below 0.25 μm. The bottom patterns of these two types of alignment marks were shown on Fig. 6.16. An example of their use is illustrated on Fig. 6.25. The first two images show the case of perfect alignment, where equal spacing are visible between the cross marks and the central graduation marks are aligned on the Vernier scales. The second two images show and example of 0.5 μm misalignment in vertical direction. The spacing at 0.5 μm segment of cross marks becomes 1 μm and is visible on the image. On Vernier scales, the second pair of graduation marks below the central ones, corresponding to 0.5 μm misalignment, are co-incident.

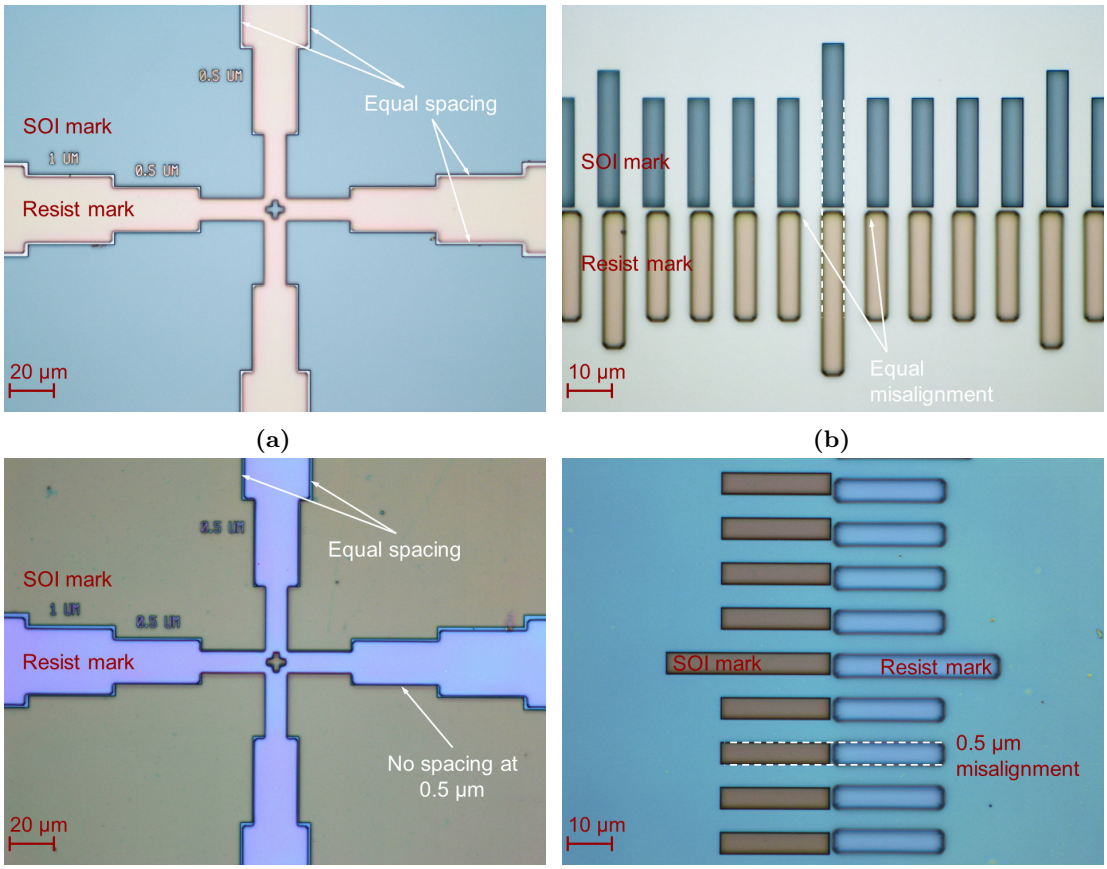


Figure 6.25: Microscope images of alignment marks after photolithography process. Perfectly aligned (a) cross marks and (b) Vernier scales for horizontal direction. (c) Cross marks and (d) in case of 0.5 μm misalignment in vertical direction.

In typical alignment procedure, the cross marks are first used for rougher alignment and compensation of rotation, and then the Vernier scales are observed for precise alignment. After sufficient practice, the accuracy $< 0.25\,\mu$m is routinely achieved.

6.6 Mesa patterning

Two mesa etch processes are done for the fabrication of VCSELs. Out of the bonded III-V epitaxy membrane individual laser devices are defined by deep mesa etching. Then, second mesa etch

is done partially to expose the bottom InP contact layer, so bottom intra-cavity contact can be formed. Patterns for these mesas are defined using previously described positive photolithography. In this section, the dry and wet etching processes for defining mesas are discussed.

6.6.1 Overview

First mesa etch can be done using dry or wet etching. Since wet etching is isotropic and would result in large undercuts, it is not appropriate for this step due to strict requirement for the device geometry. Therefore, the etching of III-V epitaxy is done using plasma dry etching in reactive ion etcher (RIE) dedicated for III-V processes. The etching is done all the way through the entire epitaxy until the SiO_2 dummy cavity layer is reached. Therefore, there is no need for careful control of the etching depth.

The second mesa is done using combination of dry and wet etching. The RIE dry etching is used most of the way and stopped once the bottom contact layer is reached, followed by short wet etching of InP contact layer to remove 20–30 nm of etched surface which would be damaged from ion bombardment. If this is not done, the ohmic contacts formed on damaged surface my exhibit higher contact resistance.

The resist is strongly affected by O_2 plasma process. Since O_2 plasma it is part of the III-V dry etching process, the resist would have poor selectivity and would not work as a good mask for this process. Therefore, a hard mask is necessary, which would not be affected by the chemistry of the III-V dry etching process. Hard mask is fabricated by depositing a layer of dielectric before lithography step. Then, the defined resist pattern is transferred to the hard mask layer by dry etching process optimized for dielectric material which would have lesser effect on the resist. The resist is then striped and fabricated hard mask is used for pattern transfer onto the III-V. The hard mask can then be selectively removed.

6.6.2 Hard mask and III-V dry etching

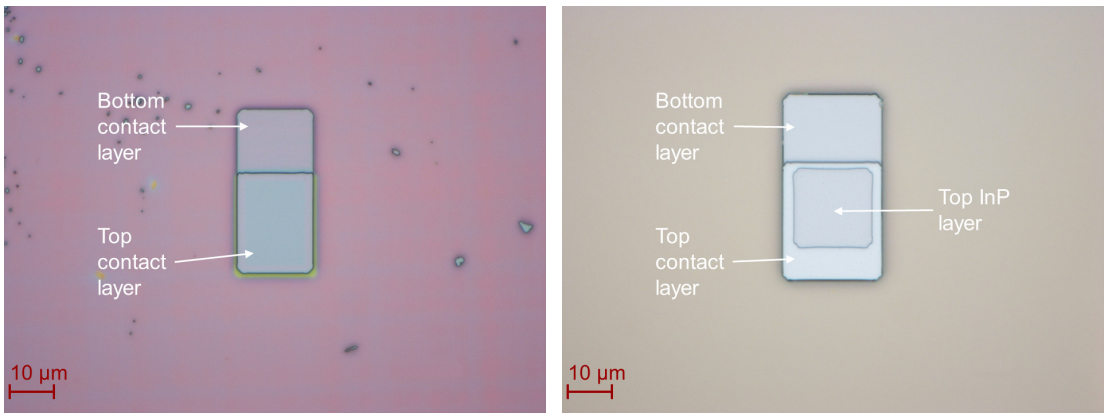
Two materials are investigated for hard mask: silica (SiO_2) and silicon nitride (Si_3N_4). Silica has higher selectivity to III-V etching process so 100 nm is enough to work as a hard mask, while silicon nitride layers used for hard mask are usually around 200 nm. Both materials can be deposited on III-V using PECVD process at 300 °C and patterned using RIE with CHF_3/O_2 chemistry. However, the RIE etching process for silica requires stronger RF power of 60 W compared with 13 W required for etching Si_3N_4 for comparable etch rate. The high power SiO_2 etch causes cross-linking of the resist, which makes it significantly more difficult to dissolve in solvent and typically requires O_2 plasma ashing to fully remove it. The other concern is the removal of the hard mask after the III-V etching is finished. Wet etching cannot be used as the exposed dummy cavity layer would be attacked underneath the III-V mesa. Therefore, the hard mask is dry etched again, which then exposes the III-V layers underneath the hard mask to ion bombardment. The high-power etch of SiO_2 would be more likely to cause damage to III-V. For these reasons the Si_3N_4 is used as hard mask material.

The III-V dry etching is done using cyclic MORIE process in RIE. This process uses CH_4/H_2 chemistry for etching InP, and more slowly InGaAs and InGaAsP compounds, with excellent anisotropy. The issue with this etching process is that a resistant polymer film is formed which reduces the etch rate, distorts the pattern and eventually completely stops the etching. To prevent this, the etching process is periodically interrupted and O_2 plasma etching is used to remove the generated polymer. Each cycle of etching consists of 2.5 min of CH_4/H_2 plasma and 30 s of O_2 plasma. Rest of the process parameters are listed in appendix A. One issue with described process is that it has very slow etch rate for compounds with high amount of aluminum. They can even be used as etch stop layers. All of the epitaxies used in this work contain compounds with Al. This is especially issue for pin epitaxy, which has InGaAlAs QWs as well as 100 nm InAlAs current blocking layer. Selective wet etching of these layers can be employed to remove these layers before dry etching is continued. However, it was experimentally proven that it is possible to dry etch through Al-containing layers, even though the etch rate is much slower.

The etching process is monitored using in situ end point detection system. Laser light with 675 nm wavelength is directed through a window on the RIE chamber onto the surface that is etched and the reflected signal is analyzed. Different materials will have different reflectivity, so the signal will have sudden change when new layer is exposed by etching. However, if the material is partially transparent then portion of the light will be reflected at each layer interface and sinusoidal change in the signal intensity will be detected due to the interference. The number of sinusoidal periods needed to completely can be calculated as $n = 2nt/\lambda$, where t is the layer initial thickness, n is its refractive index, and λ is the laser wavelength. This information can be used to estimate the remaining etching time. The laser signal pattern is recorded during first mesa etching and from it the time required for etching of each layer of epitaxy can be extracted. This information is then used to accurately stop the etching process during second mesa etch, when bottom contact layer is reached.

6.6.3 Removal of InGaAs layers

For versions v1, v2 and v3 the mesa patterning is finished by removing the InGaAs etch stop layer that was left to act as protective layer. It can be done by selectively wet etching using 1 H_2SO_4 : 8 H_2O_2 : 8 H_2O. This is done without any mask, so slight undercut etching of the active region will happen from exposed sides of the mesa. An example of fabricated mesas for v3 VCSEL is shown on Fig. 6.26a. Both contact layers are InP.



(a) **(b)**

Figure 6.26: Microscope images of fabricated mesas of (a) v3 (b) and v4 VCSELs.

For v4 version, with PIN epitaxy, the etch stop layers are removed before mesa patterning. The top layer is 200 nm of InGaAs contact layer. However, the InGaAs is not transparent around 1.5 μm wavelength, and therefore needs to be removed from the region where optical mode will be positioned. This can be done by making a mask with opening where InGaAs is to be removed, which can be done using dry or wet etching. With dry etching undercut under the mask would be avoided so that InGaAs is not removed where ohmic contact is to be formed. However, the etch process is not selective towards InP layer underneath it, so there is a danger of overetching. On the other hand, wet etching can be perfectly selective so that InP is not affected. Therefore, the etch is done with combination of dry and selective wet etching. A pattern is prepared and transferred onto a hard mask. Shallow dry etching half way through the InGaAs layer thickness is done. Then wet etching using 1 H_2SO_4 : 8 H_2O_2 : 8 H_2O is used to finish InGaAs removal. An example of fabricated mesas for v4 VCSEL with InGaAs opening is shown on Fig. 6.26b.

6.7 Proton implantation

The ion implantation as a method for defining aperture for current confinement was discussed in detail in section 3.3 of chapter 3. The implantation is used with V1 and V2 versions of the VCSELs. The target for the projected range of vacancies created by implantation is the *p*-side of the TJ. This is narrow 10 nm InGaAlAs layer in TJ1 epitaxy and 30 nm InAlAs layer in TJ2 epitaxy.

The ion species used is proton (H^+), and the implantation is done at room temperature with dose of $1 \cdot 10^{14}\,cm^2$. The ion energy necessary for targeted depth is determined using TRIM simulations of each epitaxy. The optimum energy determined for TJ1 epitaxy is 125 keV, while for TJ2 it is 100 keV. The channeling effect of the crystal lattice of the semiconductors, can influence the projected implantation range, but it cannot be simulated using TRIM software. So, to avoid the channeling effect the implantation is done with angle of 7°to the axis perpendicular to the sample surface.

As discussed in section 3.3, the combined mask of resist and Si_3N_4 is used for masking the aperture and bottom contact area from implantation. The implantation process is done in between two mesa etching processes, so hard mask used for fist mesa is reused for implantation mask. A 2 μm AZ 5214E photoresist is spin-coated and patterned, flowed by dry etching to transfer the pattern to the existing Si_3N_4 layer.

The prepared sample is packed and taken to Ion Technology Center (ITC), Ångström Laboratory, Uppsala University, where implantation is performed.

The implantation causes heavy cross-linking of the resist, which makes it exceptionally hard to remove. Striping using solvent is mostly ineffective. Long O_2 plasma ashing process is necessary to remove the resist. Any remaining resist can act as a mask during dry etch of hard mask layer underneath.

6.8 Metallization for electrical contacts

The ohmic contacts used in this work have been discussed in section 3.4 of chapter 3. A two-step metallization approach is introduced, where fabrication of metal contacts is split into two steps:

1. Ni/Ge/Au metal stack, with small amount of Au, for ohmic contact to InP;
2. thick-Au metal layer, to form contact pads which extends over larger area for easier and low resistance probing.

For both steps the patterning of metal is done using lift-off method and metal deposition is done using e-beam evaporation method.

6.8.1 E-beam evaporation and lift-off

Metallization procedure

UV lithography with negative resist AZ nLOF 2020 is used to create the resist mask, with resist being removed only where metal is to be deposited on sample surface. The masked samples are dipped in buffered HF (BHF) acid for 1 min to remove any native oxide, and then promptly loaded in e-beam evaporation chamber where thin metal layers are deposited. For *n*-type low-Au ohmic metal stack, 30 nm Ni, 50 nm Ge and 20 nm Au layers are evaporated, in that order.

The lift-off is performed by dipping the sample in Acetone for 10-20 min with ultrasonic agitation. Acetone dissolves the resist mask, which lifts off any metal that is deposited on the resist. Metal remains only in areas where openings in the mask were defined. The sample is then rinsed and dried.

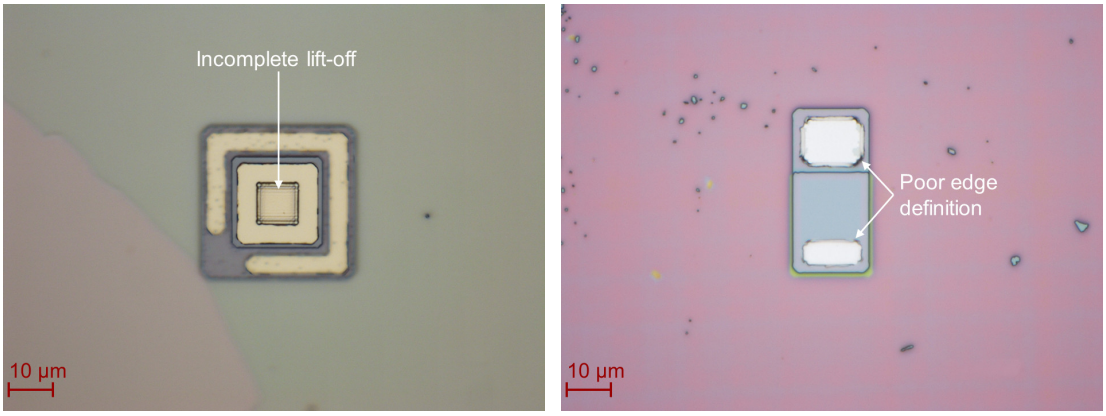
The same process is done for fabrication of contact pads. This time 10 nm of Ti is evaporated first, followed by evaporation of 280 nm of Au. The thin Ti is deposited first to improves the adhesion for Au. The thick Au layer lowers the probing resistance. The contact pads connect cover the ohmic contacts and extend beyond the device mesa over the BCB that is used to planarize the surface. The large area pads enable easy probing with contact needles during characterization.

While for VCSEL versions that use TJ both top and bottom ohmic contact are formed at the same time, in case of V4 VCSELs with PIN epitaxy n- and p-side contacts have to be fabricated separately. The n-type ohmic contact is again Ni/Ge/Au stack, but the amount of Au is increased to 100 nm since the spiking is less of an issue for only bottom contact and larger contact layer thickness. The annealing is done for this contact, and then lift-off method is repeated again for top p-type contact with Ti/Pt/Au (30/50/100 nm) metallization. Alloying is not needed for this metallization to form ohmic contact.

Lift-off issues

The issues with negative resist lithography have already been discussed in section 6.5. The biggest issue for lift-off process was the difficulty to obtain the resist with sufficient thickness and good sidewall profile. This is especially issue with thick metal layers. Two types of issues have been observed: incomplete lift-off and poor edge definition.

The incomplete lift-off is result of insufficient thickness and lack of inverted slope of resist sidewalls. This is especially issue with thicker metal layers. It is recommended for resist thickness to be at least 5 times larger than metal thickness. For thick-Au metallization that would be 1.5 μm. The large height difference and inverted slope of sidewalls are supposed to create disconnect of the metal layer. Then the solvent can penetrate underneath the metal and dissolve the resist. If this is not achieved, the metal will seal the resist and will not be lifted off. An example of incomplete lift-off is shown on Fig. 6.27a. Here the metal covers the opening in the center of the V1 version of the VCSEL. Even if the resist thickness is sufficient to cause the disconnect, if the sidewalls do not



(a) **(b)**

Figure 6.27: Microscope images illustrating the issues with lift-off. (a) Incomplete lift-off which resulted in metal covering the center of the device. (b) Lack of negative angle of the sidewall resulting in poor pattern shape and hanging "ears".

have inverted slope the metal will be deposited on them. After resist is removed, the metal will remain standing upwards and forming "ears". An example of poor edge definition of the metal is shown on Fig. 6.27b.

6.8.2 Ohmic contact annealing

The Ni/Ge/Au metallurgy requires thermal annealing to form the ohmic contact with InP. The annealing process usually consists of two stages. First, at lower temperatures the Ni reacts with native oxide of the semiconductor, and then forms intermediate Ni-InP complexes. This enables Ge to diffuse into the semiconductor and causes high doping. The temperature is then elevated further and Au reacts with In to form thermodynamically stable compound. This reaction lasts

until the temperature is reduced or Au is spent. The annealing process is commonly done using rapid thermal annealer (RTA). The temperature profile used for this process is shown on Fig. 6.28. The temperature is first ramped up to 200 °C for 60 s, and then rapidly increased to 420 °C for 15 s. To prevent the oxidation at high temperatures, the annealing is done in nitrogen atmosphere.

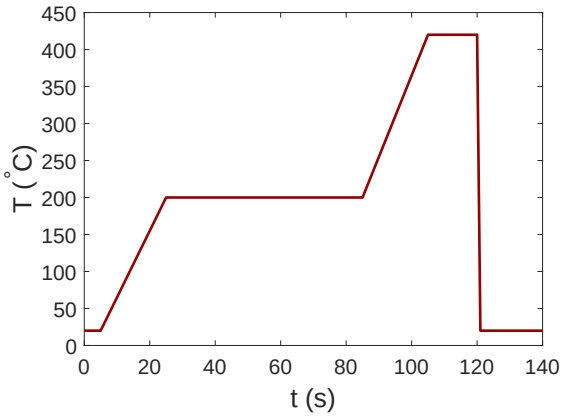
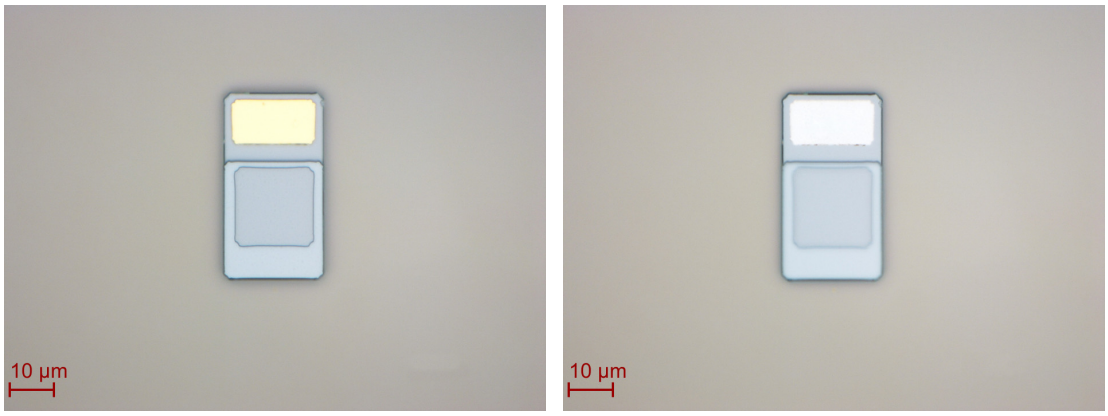


Figure 6.28: Plot of temperature versus time in RTA recipe.

Due to machine failure, early testing of the ohmic contacts was done in an oven which cannot achieve fast temperature ramps. The specific contact resistances achieved during those tests was order of magnitude larger than expected values. Later, with better optimized RTA process for contact annealing, the specific contact resistance improved and average values were around $1.1 \times 10^{-6}\,\Omega\text{cm}^2$.

The alloying of gold with semiconductor leads to color change of the metal contacts. This is illustrated on Fig. 6.29. The gold color before annealing becomes silver-like. This provides easy verification that annealing has been completed.



(a) **(b)**

Figure 6.29: Microscope images of v4 VCSELs with fabricated n-type ohmic contact (a) before and (b) after RTA.

The thermal process for ohmic contact annealing is also intended to anneal the unwanted damages created by implantation process. As discussed in chapter 3, the high resistance due to implantation in n-type InP and undoped layers is annealed at temperatures above 300 °C. The isolation created in p-type layers should reach the maximum value at the temperatures used for annealing the contacts.

6.9 Planarization for contact pads

The contact pads need to be electrically insulated from each other. Therefore, they are deposited on a non-conductive dielectric layer. Also, the height of the III-V mesa is over 1 μm, so the sample needs to be planarized so that pads are elevated closer to the ohmic contacts and metal layer doesn't break at the step between the III-V mesa and dielectric. BCB and Si_3N_4 were investigated and used for planarization. In this section both approaches will be discussed.

6.9.1 Planarization with nitride

In first design v1, the mesas are designed to be symmetrical with bottom contact surrounding the air-post mesa and top contact surrounding the DBR mirror. In order to connect top ohmic contact with its contact pad, the metal has to go over the exposed bottom contact and mesa sidewall. In order to electrically isolate the top contact pad a layer of S_3N_4 is deposited and patterned so that it covers one corner of bottom contact and mesa sidewall (see Fig. 4.1).

The thickness of the Si_3N_4 layer was chosen to be 250 nm, to avoid large step from bottom contact layer. The dry etching is used to pattern the nitride and then the contact pads are fabricated using described lift-off method.

During testing it was discovered that this method was not always successful. The PECVD deposition of Si_3N_4 doesn't planarize the surface sufficiently, and large step height between top contact layer and nitride surface occasionally resulted in disconnect of metal pad.

Instead of trying to redesign and optimize the structure it was decided to switch to planarization with BCB.

6.9.2 Planarization with BCB

Planarization with BCB is most commonly used method. The BCB has excellent planarizing property. The step heights of the mesas that are over 1 μm high are planarized down to < 100 nm at the surface of the 2.5 μm thick BCB. Furthermore, it has low dielectric constant for reduced parasitic capacitance.

Two versions of BCB are commercially available: photosensitive Cyclotene 4000 series, which can be patterned using UV lithography, and non-photosensitive variant Cyclotene 3000 series that is suitable for patterning with dry etching. The photosensitive BCB is particularly suitable for this application, since the lithography process can be optimized to result in sloped sidewalls of the pattern which would prevent disconnect of the metals that would otherwise occur at sharp steps. The non-photosensitive BCB is patterned by dry etching with resist or hard mask. Unfortunately, there was no time to try and develop suitable procedure for patterning the photosensitive BCB, so the dry etch BCB was used for fabrication of lasers, starting from version v2.

Procedure for processing BCB

The planarization step is done after ohmic contacts are fabricated to avoid damaging the III-V contact layer during dry etching of BCB. The adhesion promoter AP3000 is spin-coated and shortly baked at 150 °C, followed by spin-coating of Cyclotene 3022-46 at 5000 rpm for 40 s which results with film thickness around 2.5 μm. The sample is baked for 2 min at 150 °C to evaporate the solvent and stabilize the BCB film. It is important to remove the edge beads as they can cause lithography issues in subsequent processing. The BCB is then hard cured in oven with nitrogen atmosphere for 60 min at 250 °C. The exact temperature profile for curing process is given in appendix A.

The BCB layer thickness is chosen to be significantly larger than the mesa height for improved planarization. After curing, the BCB thickness is first reduced by doing maskless etch-back until the top of the mesa is exposed. The dry etching of BCB polymer is done using RIE with mainly O_2 plasma and small amount of fluorine species (CHF_3 is available in RIE) for the silicon present in the polymer [217]. The etching can be easily controlled using end point detection, as the signal

will abruptly change when top of the mesa is exposed. Since etch depth control is not critical, a high-etch-rate recipe is used for this step: 3:1 ratio of O_2:CHF_3 and RF power of 30 W. The etch rate is determined to be around 125–135 nm/min, when 4" carrier wafer covered with BCB is used.

Once the top of the mesa is exposed, the etching needs to be better controlled in order to reduce the BCB thickness so that it lies above the height of the active region. This should make step height between BCB surface and both contact layers approximately equal and sufficiently small to avoid metal disconnects. For more controlled etch, recipe with 4:1 ratio of O_2:CHF_3 and RF power of 10 W is used. The etch rate is determined to be around 60 nm/min. Before the final etch back, it is necessary to open the III-V area so that bottom contact is also exposed. For this purpose, a mask is fabricated. Selectivity of this etching recipe to photoresist is very poor with similar etch rate as for BCB itself. Therefore, the photoresist thickness needs to be at least twice as large as targeted etch depth. Hard mask of SiO_2 or Si_3N_4 can also be used and would have much greater selectivity, but it complicates the processing and was deemed not necessary. After the BCB is completely removed from on top of III-V, the resist is stripped and final slow etch-back is done. The etching is regularly interrupted and progress is monitored using contact profilometer.

6.10 DBR fabrication

The fabrication of dielectric DBR as top mirror is the last step in the VCSEL fabrication process flow. The DBR is made by stacking several pairs of $\lambda/4$ thick layers of high- and low-refractive-index materials. Silicon dioxide (SiO_2) and amorphous silicon (*a*-Si) are the chosen materials in this work, as they are found to offer very high refractive-index contrast. In this section the deposition and patterning of the DRB will be discussed in more details.

6.10.1 Deposition of SiO_2 and *a*-Si layers

Several methods for deposition of dielectric materials are considered for this use. In some of the previous research in our group, deposition using ion beam sputter deposition (IBSD) and electron-beam evaporator have been investigated. In this work, the main method of deposition is with PECVD process. The PECVD offers better control of the deposition thickness and is more convenient to use. The *a*-Si deposited using PECVD has high refractive index around 3.67, while refractive index of SiO_2 is measured to be around 1.46. With this high refractive-index-contrast only three pairs are sufficient for reflectivity $> 99\%$. The layer thickness is adjusted for each version and targeted wavelength. For 1.55 μm, the layer thicknesses for SiO_2 and *a*-Si are 265 nm and 105 nm, respectively. The deposition starts with SiO_2 and is followed with *a*-Si.

The deposition of *a*-Si is done using SiH_4 plasma with high RF frequency (13.56 MHz) and low power of 10 W. The temperature is 300 °C, as with all other PECVD processes. The deposition is very slow with deposition rate around 7 nm/min, but the process is not repeatable as the deposition rate tends to go down with multiple depositions. This could be caused by changing conditions in the chamber. Before starting the deposition, the PECVD chamber is preconditioned by depositing 1 μm thick SiO_2, and every deposition of *a*-Si is preceded by a dummy SiO_2 deposition. It is also important to deposit SiO_2 on the sample before *a*-Si, since the adhesion of *a*-Si to semiconductor is poor and can lead to formation of bubbles or delamination of deposited film. The poor repeatability of the *a*-Si deposition means that the deposition of whole DBR cannot be done in one run, and each layer thickness has to be verified and any deviation compensated. The layer thicknesses are measured on dummy Si sample that is placed into the chamber together with laser sample.

Before the DBR layers are deposited, additional layers of SiO_2 or *a*-Si can be deposited to fine-tune the phase of the DBR reflection to achieve resonance at the targeted wavelength. If *a*-Si is used, then thin 10 nm layer of SiO_2 is deposited first for adhesion.

As an example, the SEM image of a cross-section of 3.5-pair DBR deposited on Si substrate is shown on Fig. 6.30.

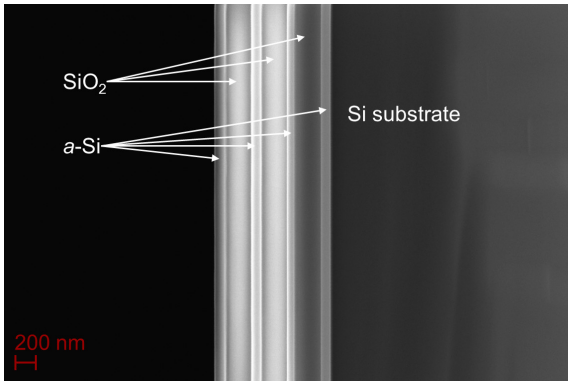


Figure 6.30: SEM image of the cross-section of a 3.5 SiO_2/a-Si pair DBR.

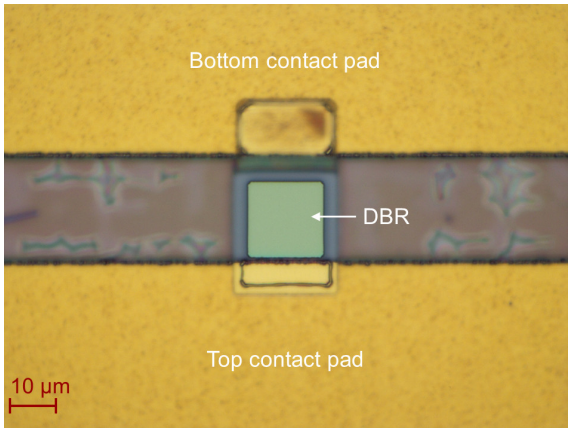


Figure 6.31: Microscope image of fully fabricated v2 VCSEL.

6.10.2 DBR mesa etching

After deposition, the DBR layers are patterned into small mesas that are positioned on top of the III-V mesas, aligned with the aperture and the HCG below it. The DBR can be patterned using lift-off method or by dry etching. Since the resist mask for lift-off would not be stable at high temperature of the PECVD process (300 °C), the dry etching method is used.

Standard UV lithography is used to create the resist mask. The thick and highly reflective DBR layer that covers the whole sample makes alignment marks almost invisible. The topology of the structures is visible; however, the alignment marks are planarized previously with BCB. This issue made accurate alignment of DBR mask challenging.

Dry etching is done using RIE process optimized for etching SiO_2, with CHF_3/O2 plasma and RF power of 60 W. This process is also capable of etching through the a-Si layers but with slower etch rate. The process can be monitored using end point detection. The interference signal changes in amplitude and period when etching switches between layers. The whole etching process takes about one hour. The selectivity of the etch to resist mask is low, so a thick resist mask is necessary. The positive AZ 5214E resist is spin-coated at low speed so that 2.3 μm resist thickness is achieved. The high power etch heavily damages the resist, so O_2 plasma ashing is necessary to strip it after the process is done.

After removing the resist, the device fabrication is finished. The Fig. 6.31 shows an microscope image of the fully fabricated VCSEL with light-green colored DBR visible in the center.

6.11 Remarks

Development of fabrication procedure, optimization of various processes and full fabrication of several generations of VCSELs has been the primary task of this project. This chapter gives a relatively short summary of the fabrication procedure that resulted from years of learning and testing.

A description of full process flow for fabrication of the lasers investigated in this work was given. It was developed with CMOS-compatibility in mind. The process flow given here is for v2 version of the VCSELs, which was the primary design in this work. However, the differences for other versions are trivial. For v1, the main difference is use of Si_3N_4 for planarization, which was replaced with BCB in following versions. Implantation step is skipped for v3 and v4, so the hard mask used for first III-V mesa etch can be reused for second mesa etch to expose the bottom contact layer. Additional patterning step is necessary for v4 version to selectively and partially remove the top InGaAs contact layer from one part of the device. The rest of the process flow is the same, with only differences in specifics of some processes, such as etching time of different epitaxies.

All the important steps and processes that are used in process flow are individually discussed in more details, with descriptions of the procedures, issues and challenges that were encountered. The detailed process flow instructions, with all the process parameters, are included in appendix A.

CHAPTER 7

Results and discussion

7.1 Introduction

Four versions of the proposed hybrid LW-VCSELs design were investigated. The specifics of the designs were presented in chapter 4. Using fabrication methods presented in previous two chapters, several samples were fully fabricated and characterized, the results of which will be presented and discussed in this chapter.

Both electrical and optical pumping was used to characterize the fabricated devices. The characterization methods and setups that were used will be described first. Then, the results will be presented for each version of VCSELs in chronological order of their fabrication over the duration of this project. In many cases, the fabrication procedure had to be modified for various reasons, such as tool breakdowns or unexpected results of the previous processes. Therefore, it is important to first present the fabrication results for each sample before the characterization is discussed.

The TJ2 epitaxy was first obtained for fabrication and demonstration of proposed design. However, the poor surface morphology meant that it was impossible to bond it with direct wafer bonding method that was developed previously. So, a new epitaxy was obtained, which is named here TJ1. The surface morphology was better for TJ1 but still not good enough for bonding. This motivated the development of adhesive bonding method which provided better results for such surfaces. The VCSELs with TJ1 were successfully fabricated and are named V1 in this thesis. However, despite mostly successful fabrication, no lasing was observed. A direct comparison of the light emission under electrical pumping between TJ1 and TJ2 epitaxies showed that issue exist with TJ1 under electrical pumping. So, the TJ1 was scraped and efforts were redirected to TJ2 again. With new design and TJ2 epitaxy, the lasers were fully fabricated once again (version V2). However, the lasing was not achieved once again. To eliminate the possibility that implantation was sabotaging the lasing, the lasers were fabricated again using TJ2 but with no implantation (version V3). No lasing was observed once again, which was unsurprising due to poor fabrication results. As a final attempt to demonstrate the lasing, a simpler PIN epitaxy was designed. The new wafers had superior surface quality and fabrication results were excellent. However, the lasing was not achieved with this version neither.

With each fabricated version, the lack of lasing results was investigated. Doing both optical and electrical characterization helped get a better idea about the possible causes. With each next version it was sought to eliminate these possible issues. The overall discussion on possible issues that were unresolved will be given at the end of this chapter.

7.2 Characterization methods and setups

In pursuit to demonstrate the efficient lasing and high frequency response, both static and dynamic measurements were designed. However, due to lack of lasing, there was no chance to do dynamic characterization and investigate the high-speed property of the design.

Static characterization was done for all fabricated samples. The electrically pumped characterization was the primary task, aiming to investigate the static properties of the laser, such as lasing spectrum, optical power, lasing threshold, thermal roll-over, mode shape, etc., but also the electrical properties of the device, such as turn-on voltage, threshold current, differential resistance, etc. The optical pumping was used to investigate the laser properties when electrical pumping failed to result in lasing. Optical pumping was intended to confirm the active region design, as well as the cavity design, without the issues that may come with electrical injection of carriers.

7.2.1 Electrical pumping method and setup

A simple microscope-based setup was used for characterization of fabricated VCSELs with electrical pumping. It is illustrated on Fig. 7.1. The sample is placed on a copper mount with thermoelectric cooler (TEC) kept at 20 °C that is mounted on the movable stage. The sample is positioned and probed using microscope with visible light illumination. The current is supplied using Keithley Instruments 4200-SCS thorough needle probes. The light output from the sample is collected through the objective lens. In order to accommodate the needles, the long working distance objectives are used (Mitutoyo Plan Apo NIR Infinity Corrected Objective 20X and 50X). The light can be directed upwards to the near-infrared (NIR) camera (Xenics Xeva) for imaging or directed out of the microscope using shortpass dichroic mirror (SP DM). A small portion of the light is transmitted through the SP DM towards the camera, while most of it is coupled into the multi-mode fiber (MMF) using piezo stage. The output is split using 3-dB coupler, with one half going into the optical spectrum analyzer (OSA) and other half into the photodiode (PD). The photodiode can record the optical power and it provides feedback signal into the piezo stage for automatic positioning of the fiber for optimal coupling.

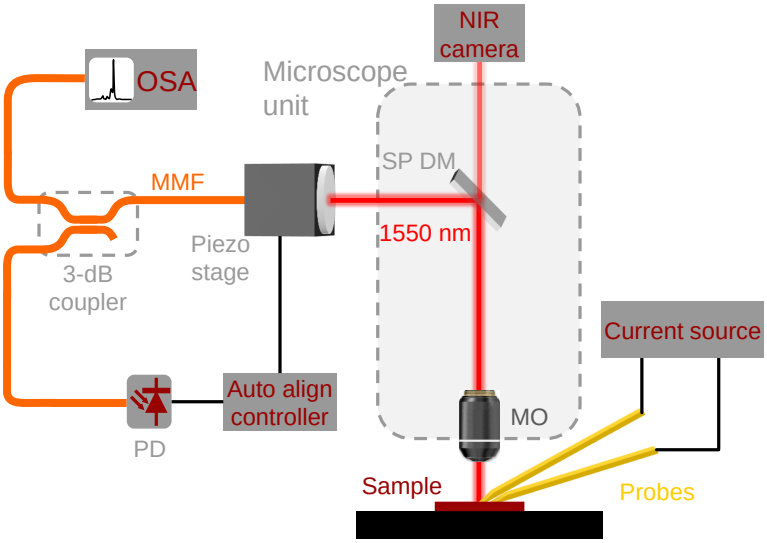


Figure 7.1: Schematic illustration of the setup for static characterization with electrical pumping.

For dynamic characterization, the vector network analyser (VNA) HP 8722C, with the frequency range 50 MHz–40 GHz would be used for measuring forward transmission S-parameter (S21). The signal would be delivered to the sample using RF probe rated for 50 GHz in ground-signal (GS) configuration. The DC bias would be delivered via bias tee from a laser diode driver.

The biggest source of losses in the setup are the objectives. At 1550 nm wavelength, the losses were -5 dB and -8 dB for 20X and 50X objective, respectively. The total loss in the setup is characterized to be around 12 dB with 50X objective.

The quick scanning of the devices for lasing is be done by applying constant current that is expected to be well above threshold and observing the light emission on the camera (by removing the SP DM from the microscope). The working devices can then be fully characterized. For full static characterization, the Keithley 4200, OSA, PD and auto align controller are all connected to NI GPIB system for easy control, data collection and analysis on computer. The measurement procedure was done as follows:

- the constant current above threshold is applied and optical power is monitored for automatic optimization of coupling using piezo stage;
- the voltage-current (V-I) characteristic is measured by sweeping the current in assigned range;
- together with V-I, the power-current (L-I) characteristic is measured using the photodiode
- the optical spectrum is recorded using OSA at set constant current levels.

The diode turn-on voltage and differential resistance can be derived from recorded V-I characteristic. The L-I characteristic gives information about the maximum optical power, lasing threshold and thermal roll-over.

7.2.2 Optical pumping method and setup

The setup for characterization with optical pumping is illustrated on Fig. 7.2. It is again microscope-based setup, where microscope is used both to deliver the pump laser light to the sample and to collect the emitted light from the sample. The pump laser wavelength is 980 nm, and it is operated in pulsed regime with a 10% duty cycle (DC) and a 5 MHz repetition rate. The pulsed operation is preferred to reduce heat generation, as the 980 nm laser is absorbed by the Si. The optical power of the pump laser is controlled using variable optical attenuator (VOA) and monitored by splitting 1% power into a power meter. The pump laser light is coupled from SMF into the microscope and directed onto the sample using longpass dichroic mirror (LP DM) which reflects wavelengths bellow 1180 nm. The microscope objective (MO) (20X or 50X) focuses the pump onto the sample. The emitted long-wavelength light is collected by the objective and directed upwards. It passes through the LP DM and is reflected by the shortpass dichroic mirror (SP DM) through the side port, where it is coupled into the MMF and taken to the OSA. If the SP DM is removed, the lasing light will be collected by the NIR camera.

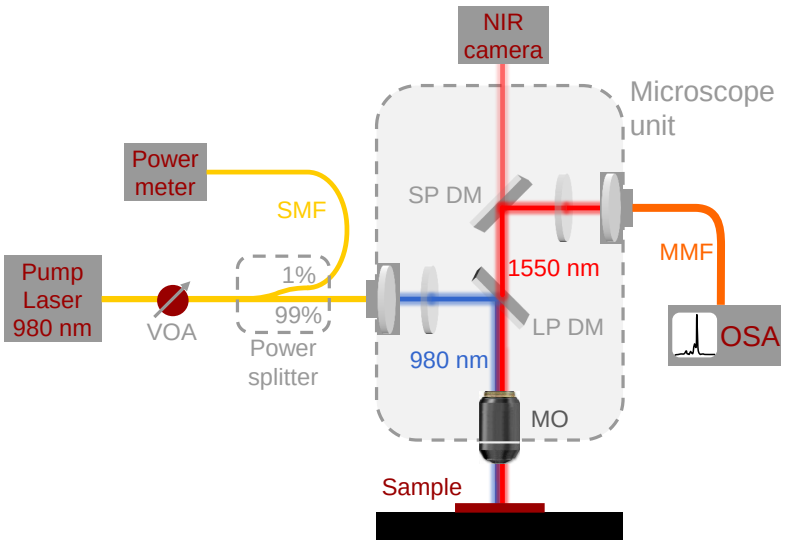


Figure 7.2: Schematic illustration of the setup for static characterization with optical pumping.

There were significant losses for the pump laser. The losses in the fibers before the light reaches

microscope were determined to be in range of 2.3–2.5 dB for powers in range of 5–30 mW. The losses in the microscope were in range of 3.1–4.4 dB, using 50X objective lens. This gives the total losses for the 980 nm pump laser in range of 5.4–6.9 dB. So, the transmittance T_s of the setup was in range of 28.8–20.3%.

The total power absorbed by the active region P_{abs} can be estimated by multiplying the pump power P_{in}, setup transmittance T_s and absorption efficiency η_{abs}. The absorption efficiency can be determined by taking approximated absorption coefficient of $10^4\,cm^{-1}$ for active layer and the thickness of the active layer. It results in 8-12% for the epitaxies used in this work. This simple estimate of the absorbed power doesn't include the reflectivity of the top mirror at the 980 nm, the absorption in the layers above the active region, the relative pump mode size and differences that come from alignment.

The equivalent threshold current I_{th} can be estimated from absorbed pump power at threshold: $I_{th} = P_{abs,th}/DC \cdot q/E_{980}$, where q is elementary charge, DC is pump duty cycle and E_{980} is the photon energy at 980 nm wavelength.

The main goal of characterization with optical pumping is to verify the optical design of the laser. In case that lasing is not achieved by electrical pumping due to issues with carrier injection, the lasing can still be achieved with optical pumping. This would confirm the optical design and enable the estimate of threshold. The pulsed operation helps with reducing the self-heating, which could prevent lasing in CW operation.

7.3 v1 VCSEL results and discussion

The first fully fabricated VCSELs were version v1 using tj1 epitaxy, symmetrical mesa design and ring contact design. Several samples were fabricated and characterized, and in this section the results will be presented and discussed.

7.3.1 Fabrication results

Design adjustments

The tj1 epitaxy structure was given in Table 4.4 in chapter 4. The PL measurement was done on a bonded sample after substrate and etch stop layer removal as the measurement before bonding would be dominated by the emission from the InGaAs etch stop layer at higher wavelengths. The gain has peak wavelength in range 1.48–1.5 μm, as shown on Fig. 7.3.

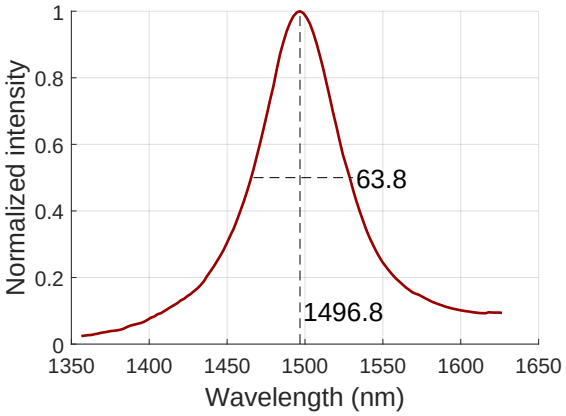


Figure 7.3: PL measurement of tj1 epitaxy after bonding and with removed substrate and etch stop layer. The gain peak wavelength is 1496.8 nm and full-width at half-maximum (FWHM) is 63.8 nm.

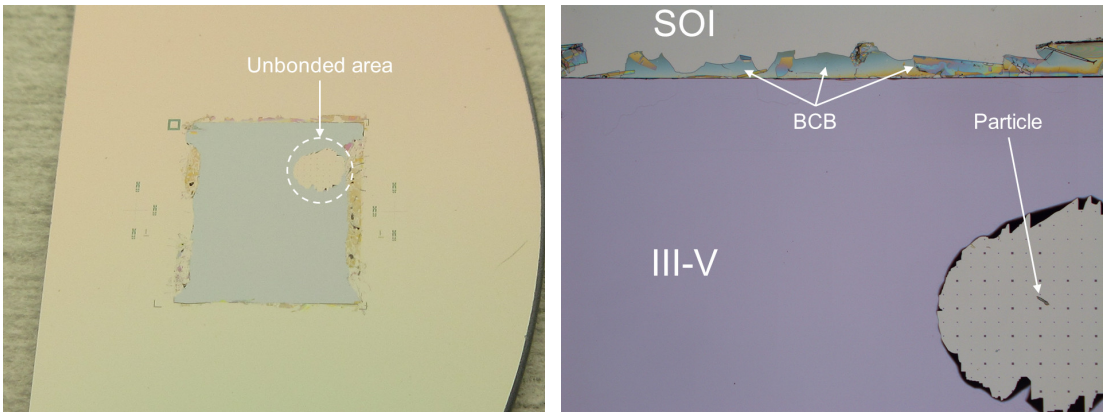
A sample was cleaved from the wafer and cross-section was examined using SEM to verify the layer thicknesses. The measurement showed relatively good agreement with design, with small

deviation of few nanometers of top contact layers and the TJ. The exception is the active region thickness that was thinner than designed, which suggested that barrier and well layers were 6.5 nm thick instead of 7.5 nm. In order to compensate the epitaxy thickness variation and match the cavity resonance wavelength to 1.5 μm where the peak gain is, the first SiO_2 layer of 4-pair DBR is adjusted to 187 nm and the SiO_2 between SOI and III-V is 184 nm.

Bonding

Samples for fabrication are cleaved from the wafer parts that contained the least amount of particles in the epitaxy. With BCB planarizing the subtle surface morphology, the bonding was mostly successful.

On one of the samples, a large area of III-V broke off during substrate removal process. This is shown on Fig. 7.4. The microscope inspection revealed a large particle that must have fallen on one of the samples during bonding preparation procedure. Thanks to the evenly distributed pressure in balloon bonder, the unbonded area was only in vicinity of the particle and rest of the sample was unaffected.



(a) **(b)**

Figure 7.4: (a) Photograph of one of the bonded samples for v1 VCSEL showing a large unbonded area. (b) Microscope image of the same sample showing a particle that was responsible for bonding issue.

In another sample, a defect was noticed in the bonding layer. It is unclear whether the defect originates from the surface embedded particles or from some contamination. In any case, the defect didn't cause debondnig during substrate removal. However, the non-uniformity of bonding layer was visible with Nomarski microscope. During PECVD process for hard mask Si_3N_4 deposition, the high temperature process caused formation of bubbles in the area of the defect, as shown on the Fig. 7.5.

These small areas, where bonding was not good enough, destroyed a relatively small number of devices. The much larger portion of the samples was intact and fabrication could still be completed with more than enough of the lasers.

Etching for bottom contact

The mesa etching was tested with dummy bonded sample before the etching was done for laser samples. These tests provided information for etching time for both first mesa etching and second partial etching. The second etching to expose the bottom contact was stopped successfully in the TJ InGaAs layer, just above the bottom contact layer. This is shown on Fig. 7.6a. With removal of InGaAs etch top layer from top of the mesa, the TJ InGaAs layer was removed also, fully exposing the InP contact layer, as shown on Fig. 7.6b. By comparing two images, the color change on top

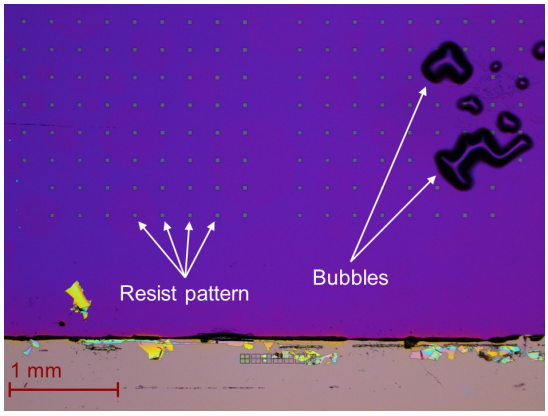
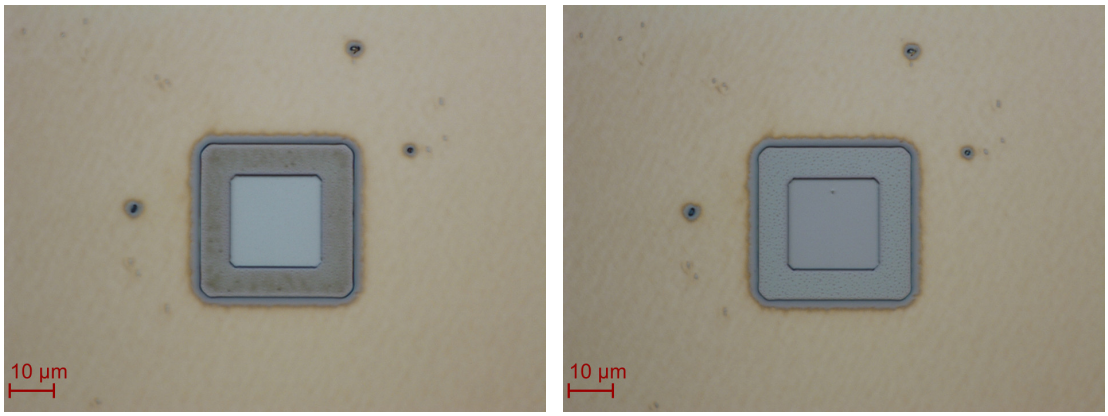


Figure 7.5: Microscope image of one of the v1 samples after PECVD process showing bubbles formed at area with defect at bonding interface.

of the mesa is noticeable, from lighter InGaAs color to slightly purple color of InP. The remains of dry etched InGaAs layer are also removed, leaving a clean InP surface ready for bottom ohmic contact.



(a) **(b)**

Figure 7.6: (a) Microscope image of the v1 VCSEL after second mesa dry etch. (b) Same device after InGaAs etch stop layer removal by wet etching.

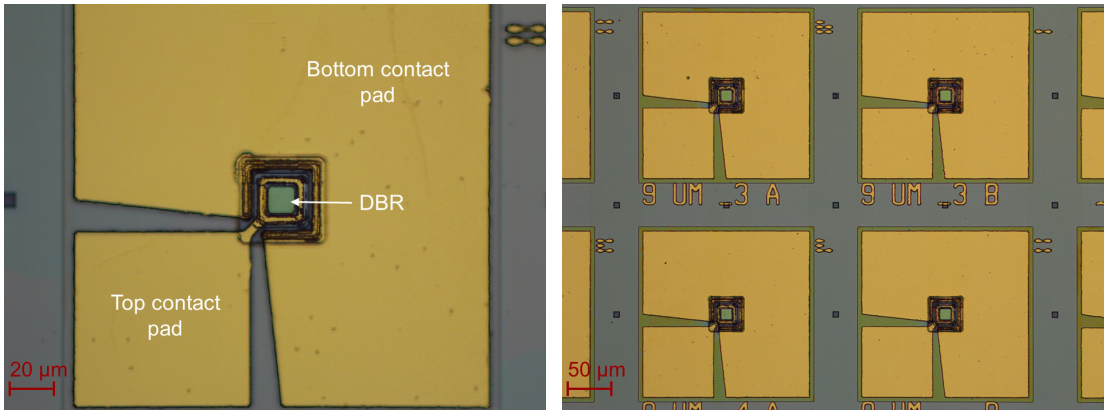
The process flow flaw

For fabrication of the v1 VCSELs, the DBR deposition and etching was done after planarization with Si_3N_4, but before the contact pads were deposited. Considering that the same chemistry is used to etch the DBR materials as for Si_3N_4 in the RIE, the slight overetch during DBR mesa etch led to etching of Si_3N_4 layer. For one sample this led to insufficient isolation of top contact pad from the lower layers on the exposed side and it caused high current leakage. To avoid this, for following samples, the fabrication of DBR is moved to after the contact pads are already formed.

The issues with negative lithography discussed before, caused issues with one sample where the lift-off for contact pads was not completely successful and many devices were left with metal still covering the central opening of the top ring contact.

Finished devices

The microscope images of fully fabricated v1 VCSELs are shown on Fig. 7.7.



(a) (b)

Figure 7.7: (a) Microscope image of the v1 VCSEL after finished fabrication. (b) Microscope image of an array of v1 VCSELs.

7.3.2 Characterization results

The characterization of several fabricated v1 samples showed no light emission with electrical pumping. Not even spontaneous emission was observed from any of the devices. The V-I measurement was done for many lasers and the typical characteristics for devices with 5, 7, 9 and 11 μm apertures are shown on Fig. 7.8. The devices show typical diode characteristic, with no visible current leakage for well fabricated samples. The turn-on voltage is in range of 0.8–0.9 V. The differential resistance is very low, varying in range of 7–25 Ω but typically around 10 Ω, leading to currents as high as 50 mA at voltage below 2 V.

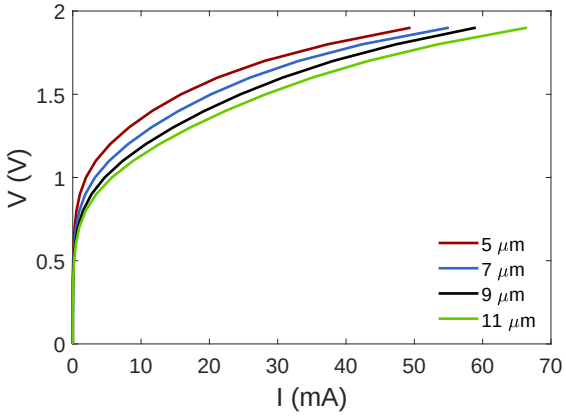


Figure 7.8: Room temperature voltage-current (V-I) characteristics of v1 VCSELs with 5, 7, 9 and 11 μm aperture.

The sample was then tested using optical pumping. Again, no light emission was observed, which is attributed to high reflection of the DBR mirror at 980 nm pump laser wavelength. Without any other option, it was decided to etch away the DBR and try characterizing the devices without it, as LEDs. The sample was returned to cleanroom and the DBR was removed with dry etching.

With electrical pumping, very faint spontaneous emission is observed now on NIR camera with long integration time. With optical pumping much stronger spontaneous emission is observed. The Fig. 7.9 shows NIR camera images of long-wavelength spontaneous emission from v1 VCSELs with varying aperture sizes under pulsed optical pumping with input power of 30 mW. The light emission is observed only within the aperture region, with some reflection on the top metal contact.

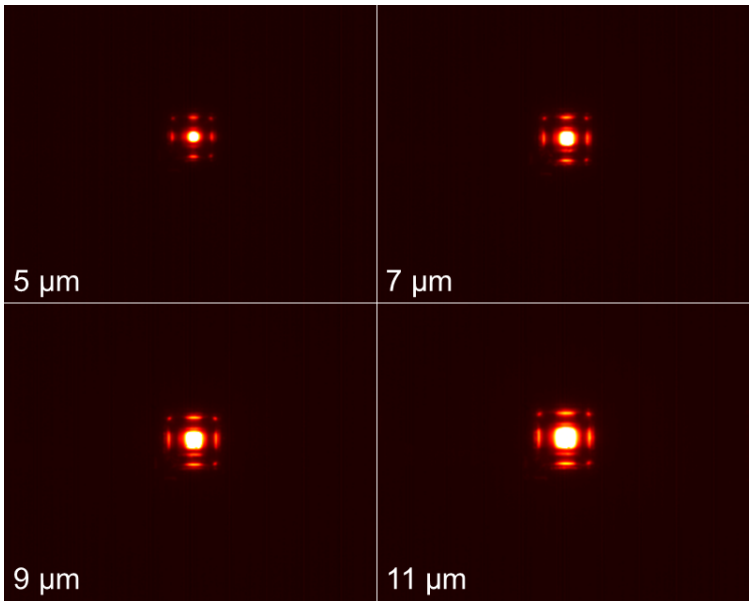


Figure 7.9: NIR camera images of optically pumped spontaneous emission of v1 VCSELs with aperture sizes of 5, 7, 9 and 11 μm. Seen with 50X objective.

The spectrum captured on OSA is shown Fig. 7.10, and it has similar shape to measured PL before fabrication of lasers.

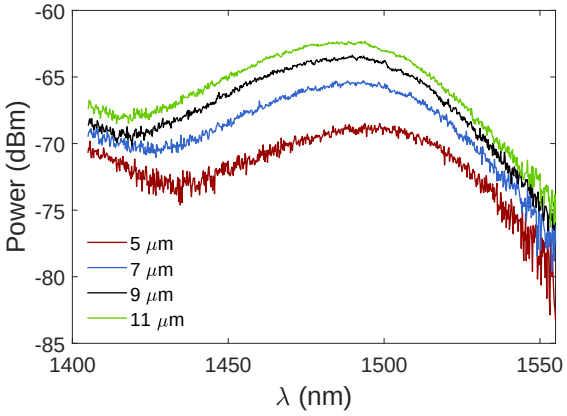


Figure 7.10: Spontaneous emission spectrum of optically pumped v1 VCSELs with aperture sizes of 5, 7, 9 and 11 μm for input pump power of 30 mW. Captured with 50X objective. The coupling losses have not been compensated.

Three samples at various stages of fabrication were tested with optical pumping and are shown on Fig. 7.11. The first image shows the light emission from an unfinished device which had first mesa defined and aperture formed by implantation. The second image shows the device with both mesas defined but no aperture and third image is fully fabricated sample without only DBR. By comparing first two images it is evident that light emission occurs only in unimplanted areas.

In case no implantation is done, the entire air-post structure is pumped and emits spontaneous emission. The pumping beam is unfocused to increase the spot diameter. With implanted devices, the light emission only occurs in small aperture region, regardless of pump spot size.

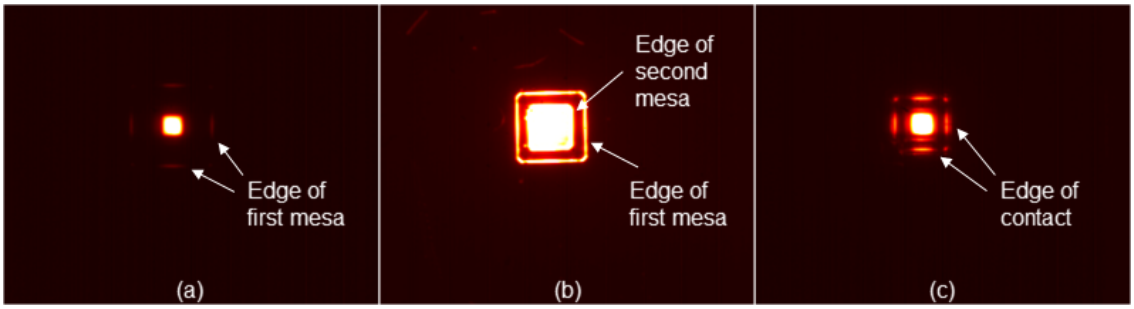


Figure 7.11: NIR camera images of optically pumped spontaneous emission of three variations of V1 VCSELs with aperture size of 11 μm: (a) unfinished device with first mesa formed and implant aperture; (b) unfinished device with both mesas formed and no aperture; (c) Fully fabricated device with DBR removed. Seen with 50X objective.

7.3.3 Discussion

The lack of light emission from implanted areas suggests that active region is damaged by the implantation and has not been recovered as was intended during thermal anneal process. The damages act as nonradiative recombination centers and no emission is achieved. Presence of such nonradiative losses would increase the threshold for lasing.

In case of electrical pumping, the spontaneous emission is again observed only within the boundary of the aperture. However, the emission is significantly weaker. With no evidence of current leakage, one possibility is that current is not directed towards the aperture sufficiently. If the implant isolation was insufficient, the current would crowd beneath the top contact and flow downwards in the shortest path. It would not be directed towards the center of the device where active region is undamaged. Therefore, the emission that is generated would be significantly smaller due to insufficient carrier injection in the aperture.

However, there is doubt whether the drastic difference in emission under optical and electrical pumping can be attributed solely to insufficient current confinement. In order to verify for sure whether the TJ1 epitaxy can provide light emission under electrical pumping, a test was designed. A simple LED devices are fabricated with TJ1 and TJ2 epitaxy for comparison and characterized with electrical pumping.

7.4 Comparison of TJ epitaxies

To verify whether the TJ1 epitaxy is capable of emitting light under electrical pumping, a simple LED devices are fabricated. The devices are fabricated without bonding by doing a partial mesa etch to expose the bottom contact layer. The contacts are formed on top of the mesa and on the exposed contact layer. The mesa is designed to narrow down in the area between two contacts to achieve carrier confinement. No implantation nor planarization is done for this device. The minimalistic fabrication eliminates any possibility of it affecting the device properties.

For comparison, the LEDs are fabricated using both TJ1 and TJ2 epitaxy as a reference. One such fabricated device is shown on Fig. 7.12a. The Figs. 7.12b and 7.12c show NIR camera images of the LED made from TJ1 and TJ2 epitaxy, respectively, with applied 3 V voltage at the contacts. The spontaneous emission from TJ2 LEDs clearly observed, with highest intensity in the narrow mesa region just between the contacts. On the other hand, the spontaneous emission from TJ1

LEDs is very faint. The integration time of the camera was increased 10 times to just see any emission at all around the contact.

(a) **(b)** **(c)**

Figure 7.12: (a) Microscope image of the test LED structure. (b) & (c) NIR camera images of electrically pumped test LED made from TJ1 and TJ2, respectively. Both images are captured for applied 3 V. The integration time for image (b) is 10 times longer than for image (c). Seen with 20X objective.

The voltage-current characteristics of both types of devices are shown on Fig. 7.13. The clear diode behavior of V-I curve shows that the devices are fabricated as intended and lack of light emission in TJ1 case is not due to issues with fabrication. The differential resistance of TJ1 is unexpectedly small, around 3.5 Ω, while the TJ2 has differential resistance of around 28.5 Ω.

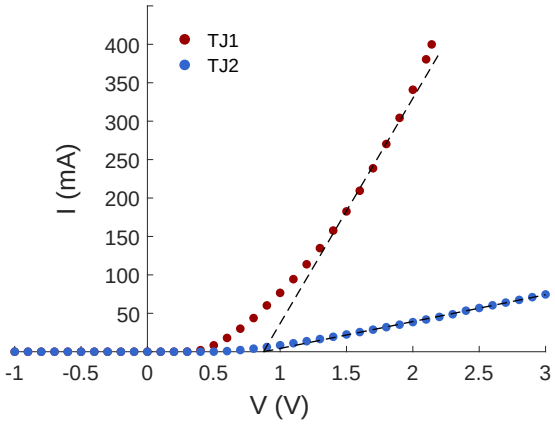


Figure 7.13: V-I characteristics of LEDs made from TJ1 and TJ2 epitaxy. The linear fit is used to determine the differential resistance of the devices.

From this test it can be concluded that TJ1 epitaxy may have a issue with design which prevents the light emission with electrical pumping. On the other hand, the TJ2 epitaxy showed good emission and more consistent electrical properties. So, the research is returned to TJ2 epitaxy.

7.5 v2 VCSEL results and discussion

Following the failure of the TJ1 epitaxy, the VCSELs were redesigned for TJ2 epitaxy. Apart from the change in epitaxy, based on the experiences with fabrication of v1 VCSELs, the design was changed for v2 version of the VCSELs, as outlined in chapter 4. The design was simplified, with asymmetric intra-cavity arrangement of contacts, reduced mesa size and BCB planarization. The fabrication flow was somewhat easier with less possibility of error.

Even though the characterization of v1 VCSELs showed that implantation induced damage in active region was not annealed as planned, it was not possible to judge how much it would influence

the performance of the laser and would the gains in the confinement outweigh the additional losses. Therefore, the implant apertures were kept for this version also.

7.5.1 Fabrication results

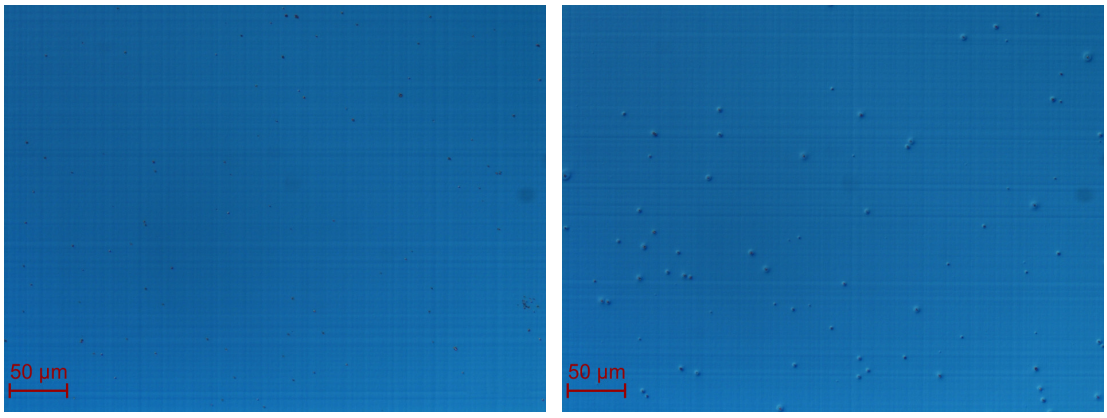
Design adjustments

The TJ2 epitaxy structure was given in Table 4.5 in chapter 4. The cross-section investigation using SEM showed some deviations from design, with slightly thicker active region and 30 nm thinner bottom contact layer. The TJ2 epitaxy was initially intended for somewhat different VCSEL design. To adapt it for this design, epitaxy is modified by etching around 132 nm of bottom contact layer before bonding. This leaves around 300 nm of bottom contact layer. This was done by wet etching using 1 HCl : 4 H_3PO_4 : 1 H_2O. Dummy test samples from same epitaxy were fabricated with hard mask structures. By dipping the test sample into the etchant and measuring the step height of the masked structures using surface profilometer, the etch rate was determined to be around 2 nm/s. With estimated etching time, the clean sample intended for laser fabrication was dipped together with test sample. In this way the etch can be precisely characterized and controlled.

Furthermore, the dummy cavity silica layer deposited on the III-V sample before bonding is determined to be 200 nm, and to tune the phase condition for cavity resonance wavelength of 1.545 μm, additional layer of 92.5 nm a-Si is deposited before the DBR pairs (with 10 nm of SiO_2 first for adhesion).

Bonding

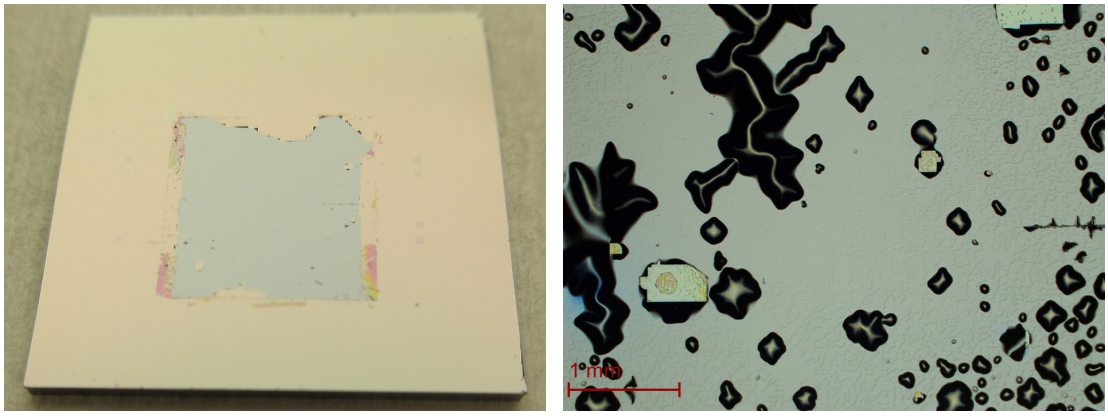
The wet etching of the bonding surface had an undesirable consequence. The wet etching lifted-off some portion of smallest particles embedded in the very surface of the epitaxy, but it didn't affect the numerous bigger particles. As a results the particles became more pronounced like small islands protruding on the surface, as illustrated on Fig. 7.14, which had drastic effect on the bonding.



(a) **(b)**

Figure 7.14: Nomarski microscope images of the TJ2 epitaxy (a) before and (b) after wet etching of the surface.

One sample was relatively successfully bonded. As shown on Fig. 7.15a, the most of the epitaxy survived the substrate removal process, with only small unbonded areas near the edges. However, the closer look under the microscope revealed a large amount of bubbles and cracks. Furthermore, a pattern was visible using Nomarski microscope which originate from non-uniform BCB bonding layer. Smooth areas with uniform BCB were observed only on the corners, where BCB is thicker because of the edge beads.



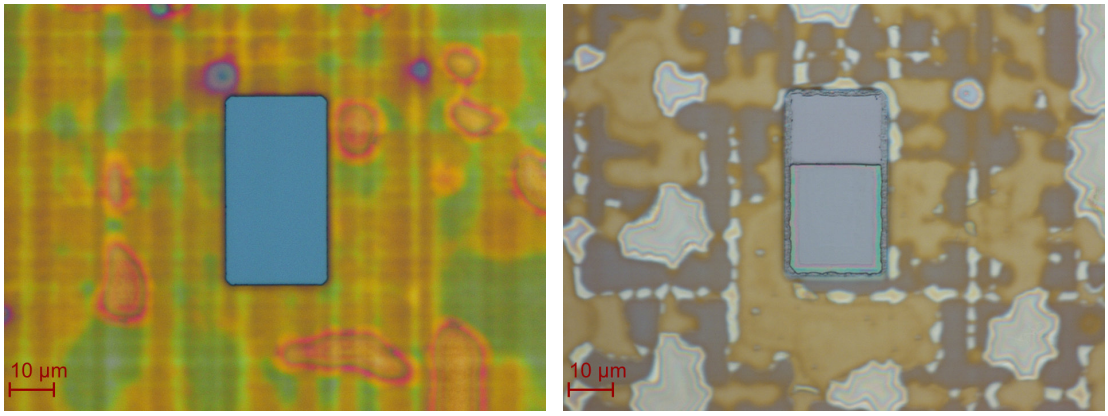
(a) (b)

Figure 7.15: (a) Photograph of the bonded sample for v2 VCSEL showing a mostly bonded area. (b) Microscope image of the same sample showing large number of bubbles and cracks. A random pattern originating from bonding layer is visible under the remaining III-V.

Despite that large portion of the epitaxy was ruined, due to the small size of the devices, large number of them were placed outside of unbonded areas and bubbles. With sufficient high number of potential devices, the fabrication was continued.

Mesa etching

At the time of fabrication of this sample, the CH_4/H_2 gasses were not available in the cleanroom due to technical issues. Therefore, the mesa etching could not be done using RIE tool. Instead the inductively coupled plasma (ICP) RIE tool is used with $Cl_2/Ar/N_2$ chemistry for etching InP-based materials. This process has higher etch rate compared with MORIE process and is performed at elevated substrate temperature of 180 °C. The SiO_2 is used for fabricating hard mask, since it has higher selectivity. An example of resulting III-V mesa (still covered with hard mask) is shown on Fig. 7.16a. The color variation from non-uniform bonding layer is visible around the mesa.



(a) (b)

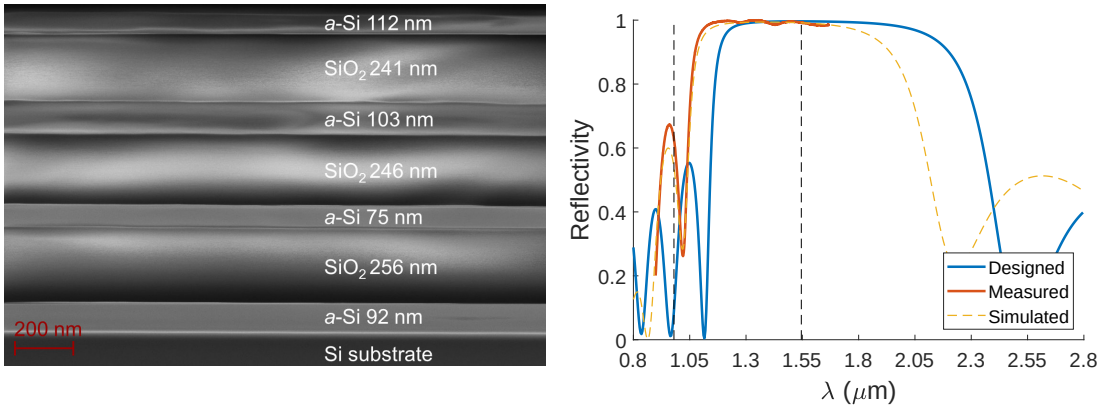
Figure 7.16: (a) Microscope image of the v2 VCSEL after first mesa dry etch still covered with hard mask. (b) Same device after wet etching is done for second mesa. The significant undercut from isotropic etching is observed.

During testing of ICP etching process, it was found that it leaves residuals on the etched surface,

most likely originating from reaction with the Si substrate. This was not a problem for first mesa etch, where all of III-V is removed from unmasked areas, and mask protects the remaining mesa surface. However, it would be an issue for second mesa etching, where such residuals would prevent good ohmic contact. For that reason, it was decided to attempt to do second mesa etch by wet etching only. The sulfuric acid/hydrogen peroxide based etchant was used to remove InGa(Al)As layers and diluted hydrochloric acid was used to remove top InP contact layer. At each step, the etching progress was characterized using profilometer. One example of device after wet etching was completed is shown on Fig. 7.16b. The isotropic nature of wet etching resulted in significant undercutting of the air-post structure. However, any exposed bottom contact layer on the sides of the air-post was covered with BCB after planarization.

DBR deposition

The deposition process of the DBR layers was unstable due to technical issues with the PECVD tool. It resulted in deviation of several layers from targeted thicknesses. The layer thicknesses are measured on cleaved dummy sample using SEM, as shown on Fig. 7.17a, and reflectivity of the DBR is characterized using PL measurement tool. The Fig. 7.17b shows comparison of measured reflectivity spectrum and targeted spectrum. The simulated spectrum based on measured thicknesses is also shown. The high reflectivity is still achieved at targeted wavelength, but the entire spectrum is blue-shifted slightly. This results in one of the side-peaks matching the pump laser wavelength of 980 nm, resulting in $> 60\%$ reflectivity.



(a) **(b)**

Figure 7.17: (a) SEM image of cross-section of DBR deposited for v2 VCSEL. (b) The plot of measured and simulated reflectivity spectrum.

Rest of the fabrication went as expected and the microscope image of fully fabricated v2 VCSEL is shown on Fig. 7.18.

7.5.2 Characterization results

The Fig. 7.9 shows NIR camera image of light emitted from v2 VCSEL under electrical pumping with current at which maximum output is achieved. Only spontaneous emission is observed, emitted from around the DBR and scattered on the mesa edges, while there is no light emission from the DBR. For comparison, the second image on Fig. 7.19 shows emission from a LED fabricated in same way as VCSEL but without the DBR. In case of LED, emission is observed from the aperture region in the center of the device.

The voltage-power-current characteristics have been measured for all of the working deices. The Fig. 7.20 shows typical results for VCSELs with aperture sizes of 5–13 μm. The V-I curves show expected diode behavior, with differential resistance determined to be in range of 200–150 Ω, respectively, and slightly high turn-on voltage around 1 V.

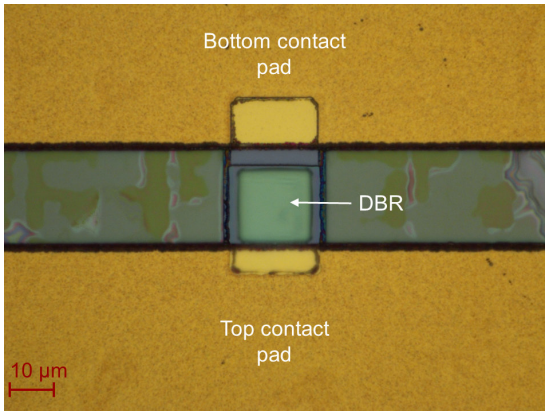


Figure 7.18: Microscope image of the v2 VCSEL after finished fabrication.

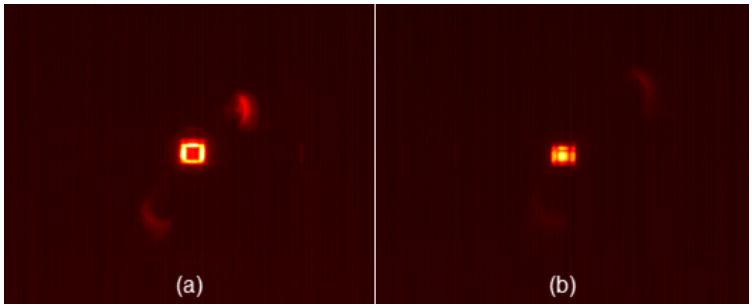


Figure 7.19: NIR camera images of electrically pumped spontaneous emission of v2 (a) VCSEL and (b) LED with aperture size of 11 μm at current for maximum output power. Seen with 20X objective.

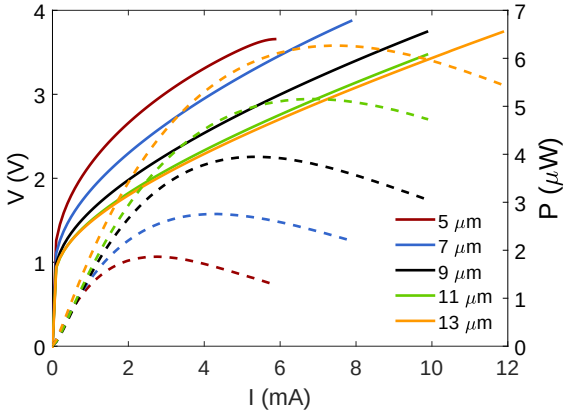


Figure 7.20: Voltage-power-current characteristics of v2 VCSELs with 5, 7, 9, 11 and 13 μm aperture. The solid lines show voltage versus current and dashed lines show corresponding optical power.

The optical power of spontaneous emission is measured using photodiode. The losses in the setup are compensated for the plotted curves. With increase of the aperture size, the power increases and thermal roll-over occurs at higher current levels. Unfortunately, due to the high losses in the setup, it was not possible to observe the optical spectrum on the OSA.

Optical pumping of the v2 sample was done in effort to determine whether the lack of lasing is

due to issues with electrical injection or due to the optical properties of the fabricated laser. The Fig. 7.21 shows NIR camera images of long-wavelength spontaneous emission from v2 VCSELs with varying aperture sizes under pulsed optical pumping with input power of 30 mW. Only spontaneous emission is observed again, only around the DBR and scattered on the mesa edges, the same as with electrical pumping. The bottom right image shows emission from the LED with 13 μm aperture. Like with electrical pumping, the emission is limited in the aperture region.

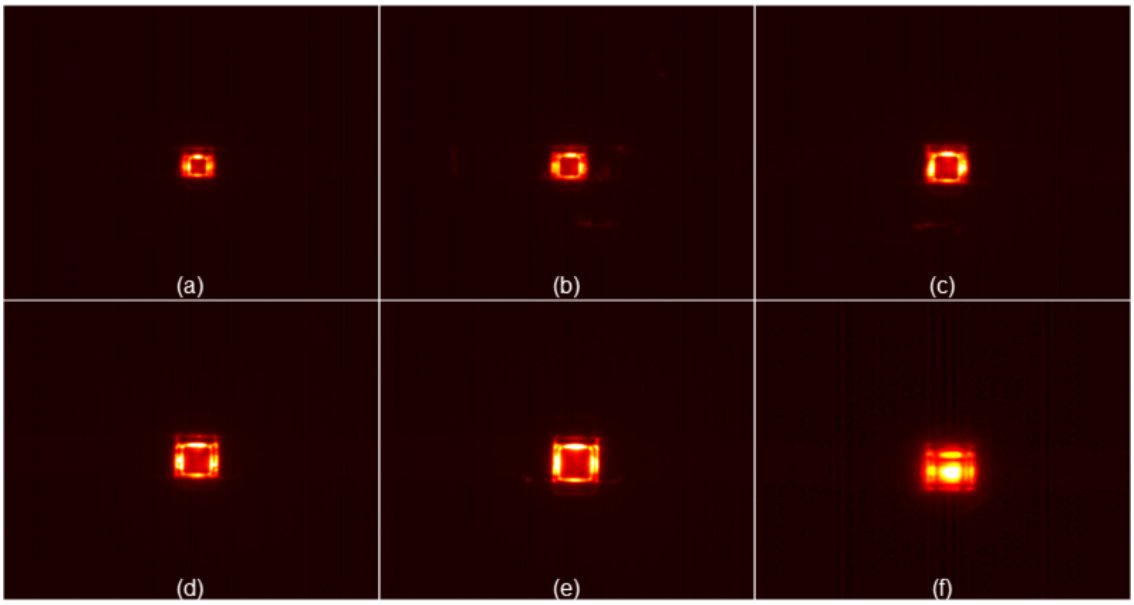


Figure 7.21: NIR camera images of optically pumped spontaneous emission of v2 (a)–(e) VCSELs with aperture sizes of 5, 7, 9, 11 and 13 μm, and (f) LED with aperture size of 13 μm at 30 mW input pump power. Seen with 50X objective.

Optical spectrum of emission under optical pumping with input power of 30 mW was captured with OSA. The Fig. 7.22 shows spectrum of several typical VCSELs. The power levels are low, with broad spontaneous emission about 5-10 dBm above the noise level. A small peak is observed for many devices, most commonly located at wavelengths around 1.6 μm. The peak height is less than 5 dB higher than the rest of the spectrum and much broader than a lasing peak, suggesting that it is amplified spontaneous emission (ASE), below the lasing threshold. Only one device was found to have ASE peak near the 1.55 μm (the green colored line on the Fig. 7.22).

7.5.3 Discussion

As with version v1, the v2 VCSEL showed no lasing with both electrical and optical pumping. However, in this case the spontaneous emission is observed with electrical pumping also. In fact, the images on Fig. 7.21 are obtained with 4 times longer integration time of the NIR camera compared with images on Fig. 7.19, suggesting that emitted power is stronger with electrical pumping.

The differential resistance of the lasers is higher than expected, which is attributed mostly to TJ series resistance and small contact size.

With both electrical and optical pumping of LED devices, with no top DBR, the emission is observed only within the aperture region. It can be assumed that same happens for VCSELs, but the DBR covers the aperture region so only light that is scattered at the edges of the structure is observed. The same conclusion as with v1 can be drawn: the active region remains damaged in

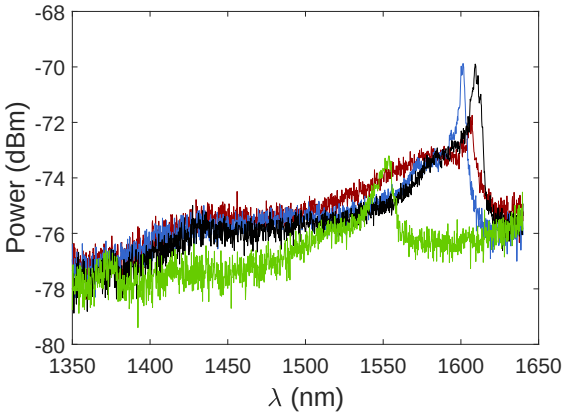


Figure 7.22: Spontaneous emission spectrum of several optically pumped v2 VCSELs with aperture sizes of 9, 11 and 13 μm for input power of 30 mW. The coupling losses have not been compensated. 50X objective is used.

region where implantation is done and the nonradiative losses contribute to the increase of the lasing threshold.

The optical pumping gave evidence of spontaneous emission being amplified, however the resonance wavelength is significantly shifted to longer wavelengths. The three most likely causes for the resonance shift that come from fabrication are: (a) the DBR reflection phase is changed due to deviation from design, (b) the deviation of bonding layer thickness and (c) insufficient etching of bottom contact layer before bonding. The numerical simulations of the cavity resonance, with measured DBR layer thicknesses taken into account, suggest that resonance wavelength would be shifted by around 10 nm to shorter wavelengths, with some decrease in quality factor. However, this doesn't agree with observed experimental results. This suggest that other causes have more significantly affected the cavity resonance. The bonding layer non-uniformity has been observed, but it was not possible to accurately characterize it without destroying the sample. The InP etchback was done by wet etching and characterized by measuring on dummy test sample that was etched together with real sample. This method may not be sufficiently accurate.

Therefore, from this discussion it can be concluded that the lack of lasing can be attributed to combination of reduced quality factor, resonance shift to longer wavelengths away from gain peak and increased losses from damaged active region outside aperture. The thermal roll-over becomes dominant effect before the lasing threshold could be reached. It should be also noted that the DBR has over 60% reflection at pump laser wavelength, which reduces the pumping efficiency significantly.

While there could possibly be other reasons for poor performance that haven't been identified in this characterization, the next VCSEL fabrication aimed at solving the issues that were found with v2 VCSELs.

7.6 v3 VCSEL results and discussion

The research continued with tj2 epitaxy, despite low boding yield, as no new epitaxy was obtained at this time in the project. With v3 version of the VCSEL, the goal was to try and eliminate the issues that were observed during fabrication and characterization of previous version. One big design change that was introduced in v3 version is that no implantation was done for creating the aperture to avoid damaging the active region. This would lead to reduction of the confinement factor, which will increase the threshold and degrade the performance but also reduce the differential resistance. As discussed in chapter 4, to improve the confinement in absence of aperture, the design is revised to reduce the size of the air-post structure. However, for comparison purposes, only half of the VCSEL array in the design is redesigned, while other half is left with v2 design.

Since no aperture is defined, the devices with different sizes are referred to by the targeted mode size defined by the grating and DBR sizes.

7.6.1 Fabrication results

At the time the fabrication of v3 VCSELs started, there were only few pieces of TJ2 epitaxy available. Furthermore, these pieces were cleaved from outer part of the wafer and they had even higher density of particles. Only two samples were bonded and they were fabricated together.

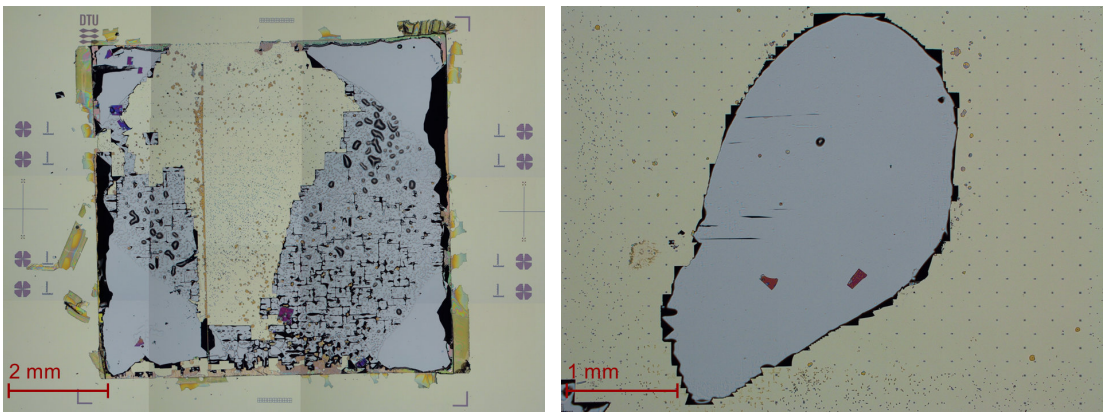
Design adjustments

The design of the v3 VCSELs is the same as for v2 and, just like in previous fabrication, it is necessary to etch back the bottom InP contact layer for 132 nm before bonding. Considering the poor morphology left after wet etching, for this fabrication dry etching is used for this process. This gave better control of etching depth and more reliable measurement as the test sample and laser sample can be placed together right next to each other in the etching chamber. The resulting surface did not display increased morphology despite presence of particles.

Bonding

Despite eliminating the issue with etchback, the results of bonding were even worse than for v2 sample. The Fig. 7.23a shows a composite microscope image of the first bonded sample. Large part of the epitaxy completely detached during substrate removal. The remaining part had large amount of bubbles and cracks. The non-uniformity of BCB layer is visible using Nomarski microscope. The exception were the corners of the III-V film which remained smooth and without defects, thanks to the thicker BCB at the edge beads. Despite the numerous defects, a relatively large number of devices could still be fabricated on remaining III-V areas.

The second sample is shown on Fig. 7.23b. Only a small area in the central part of the sample remained after substrate removal. However, apart from a few cracks, the epitaxy looked mostly free of bubbles and defects. Furthermore, the BCB layer seems to have remained uniform, as no pattern was observed. Several tens of VCSELs would be positioned in the area that is still covered with III-V. With no remaining samples of the epitaxy, it was decided to proceed with full fabrication on both of these samples, as a sufficiently large number of devices could still potentially be fabricated successfully.

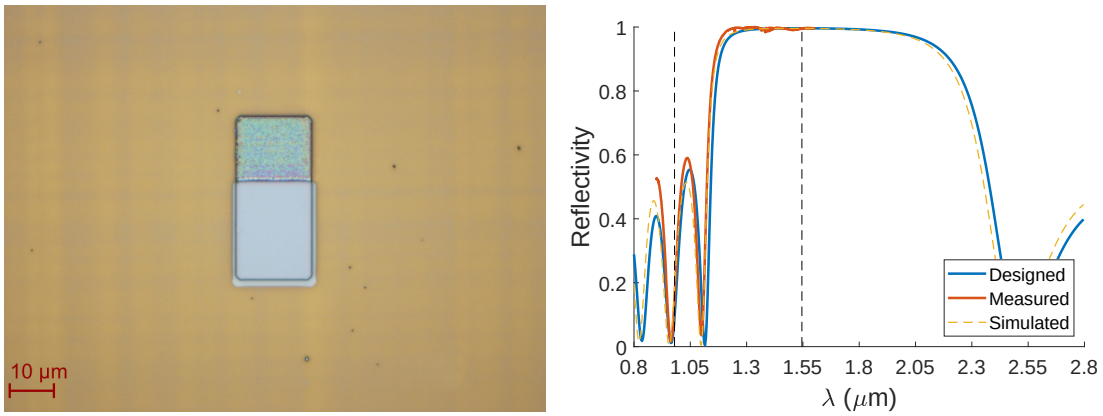


(a) **(b)**

Figure 7.23: Microscope images of two bonded samples for v3 VCSEL.

Mesa etching

The dry etching was once again used for etching of III-V mesas and the etching went mostly as expected. The only issue occurred with second mesa etch for second sample as the etching was not stopped on time and bottom contact layer was thinned down. Measurements with profilometer showed that approximately 200 nm of contact layer remained. The Fig. 7.24a shows a microscope image of one such device. The over-etched bottom contact layer is rougher and colorful due to small thickness.



(a) **(b)**

Figure 7.24: (a) Microscope image of the v3 VCSEL from second sample after second mesa dry etch. (b) The plot of measured and simulated reflectivity spectrum of the DBR deposited for v3 VCSELs.

Finished devices

Rest of the fabrication went mostly as expected. The dry etching of BCB resulted in rougher surface for first sample. This then caused darker color of the metal that is deposited on it due to scattering of light.

In order to avoid deviations during the DBR layers deposition, the PECVD deposition of each layer is done and characterized separately. As a result, excellent agreement of measured reflectivity spectrum and targeted spectrum is achieved, as illustrated on Fig. 7.24b.

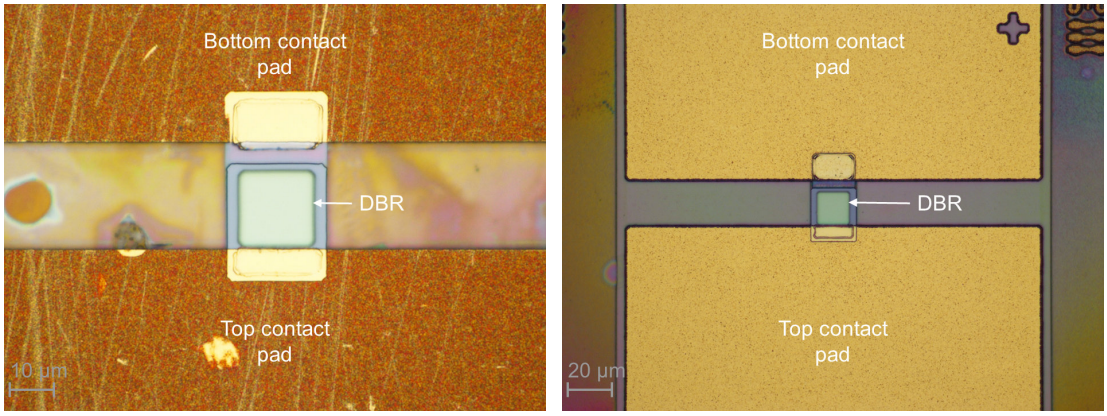
The fully fabricated v3 VCSELs are shown on Fig. 7.25. The rougher surface of the BCB on first sample causes darker color of the metal that is deposited on it.

7.6.2 Characterization results

The characterization of second v3 sample with electrical pumping showed exceptionally high series resistance of the device, reaching up to 100 kΩ. This is the result of over-etch during second dry etching step where bottom contact layer was significantly thinned down. Therefore, only negligibly small spontaneous emission is observed.

The first sample showed similar voltage-power-current characteristics as was demonstrated for v2 VCSELs. Only spontaneous emission is observed again, emitted from around the DBR and scattered on the mesa edges, while there is no light emission from the DBR. The Fig. 7.26 shows typical results for VCSELs with aperture sizes of 5–13 μm. The electrical characteristics are similar, although less consistent differential resistance is observed due to somewhat poorer metallization. The measured optical power (compensated for losses in the setup) is about 3 times lower compared with power observed for v2 VCSELs.

An interesting effect was observed during electrical characterization of first v3 sample. For some of the devices that were tested, the V-I characteristic initially showed larger turn-on voltage



(a) **(b)**

Figure 7.25: Microscope images of the v3 VCSELs after finished fabrication on (a) the first sample and (b) second sample.

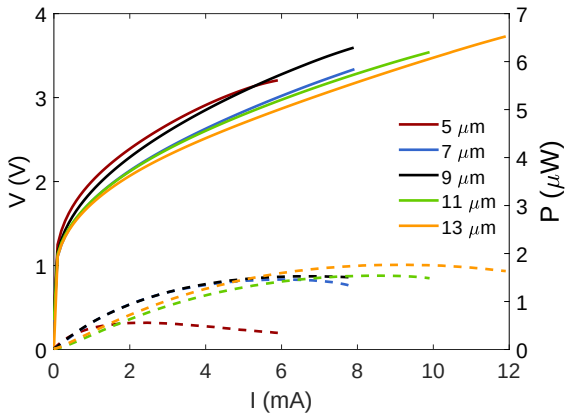


Figure 7.26: Voltage-power-current characteristics of v3 VCSELs for 5, 7, 9, 11 and 13 μm mode size. The solid lines show voltage versus current and dashed lines show corresponding optical power.

was around 2.1 V and once a certain pumping current level is reached the measured voltage would suddenly drop about 1 V. During repeated measurement, the V-I characteristic would look as expected, with turn-on voltage around 1 V similar to other devices that were measured. This effect is illustrated on Fig. 7.27, where an example of two such measurements are plotted. The change also affects the light emission, as the optical output is stronger during first measurement and drops after the characteristic changes. The Fig. 7.28 shows NIR camera images of light emitted from a v3 VCSEL under electrical pumping before and after the change in V-I characteristic. The images are captured for currents at which maximum output is achieved for each case.

It is unclear what is the cause of this effect. Any following measurement on the same device after this change would follow the new characteristic and effect is irreversible. It is evident that it happens due to self-heating effect, once the high enough voltage is reached. It cannot be caused by changes with ohmic contacts, such as additional alloying due to high local temperature at the metal-semiconductor interface. The change in resistivity would give different differential resistance, and any metal diffusion through the diode junction would give high current leakage. The change in turn-on voltage suggests that change happens to the diode structure itself.

Optical pumping of the v3 also showed similar results to v2 VCSELs. The Fig. 7.29 shows NIR camera images of long-wavelength spontaneous emission from both samples of v3 VCSELs

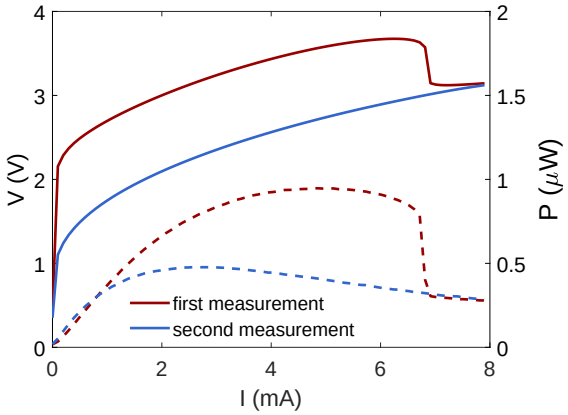


Figure 7.27: Repeated measurement of voltage-power-current characteristics of the same v3 VCSELs.

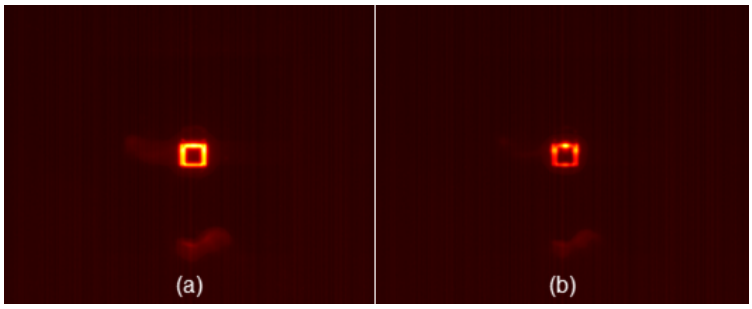


Figure 7.28: NIR camera images of electrically pumped spontaneous emission of v3 VCSEL for 13 μm mode size (a) during first measurement and (b) during second measurement at current for maximum output. Seen with 20X objective.

for 5 μm mode sizes under pulsed optical pumping with input power of 30 mW. The light emission is observed only around the DBR and scattered on the mesa edges, the same as with electrical pumping. The third image shows emission from a LED device. In absence of implantation, the active region is undamaged and light emission is observed from whole air-post part of the structure, as was seen with unfinished v1 devices previously.

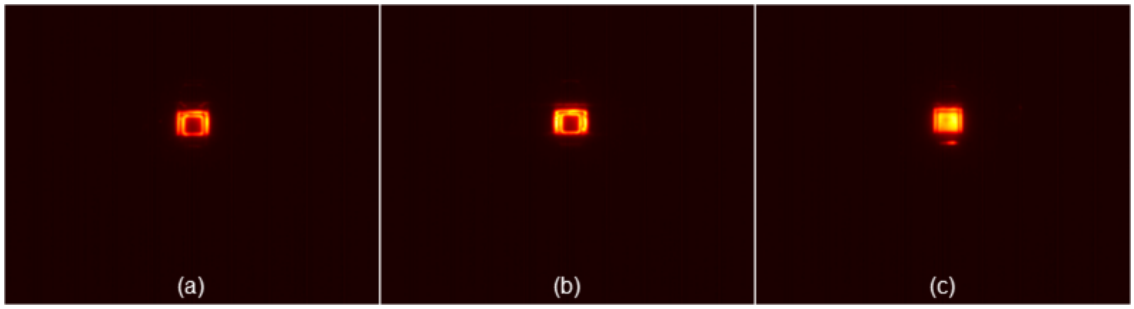


Figure 7.29: NIR camera images of optically pumped spontaneous emission of v3 VCSELs for 5 μm mode sizes (a) from first sample and (b) second sample; (c) v3 LED. Input pump power is 30 mW. Seen with 50X objective.

Optical spectrum of emission under optical pumping with input power of 30 mW was captured

with OSA. The Fig. 7.30 shows spectrum of several typical VCSELs. The second sample showed somewhat higher optical output than first sample, which can be attributed to better quality of the III-V after bonding. However, the overall output power is weaker than v2 VCSELs, even though the spectrum power levels are higher. This is attributed to lower coupling losses, which have not been accounted for in plotted results. The similar ASE peak is observed in the spectrum but only in for smaller devices, with mode sizes of 5 μm (red line) and 7 μm (blue line). This time the peak wavelength is around 1480–1490 nm. Only one device was found to have ASE peak near the 1.54 μm (the green colored line on the Fig. 7.30). The larger devices show only broad spontaneous emission spectrum (black line for 13 μm size device).

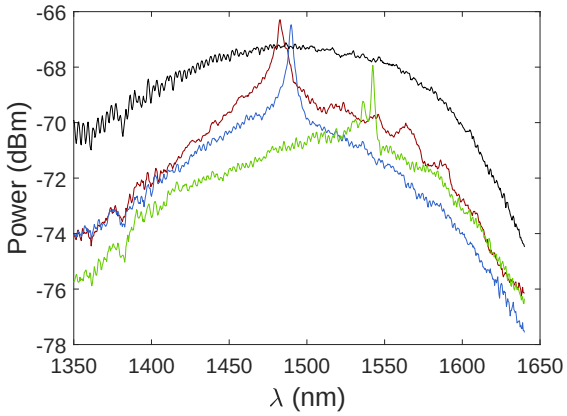


Figure 7.30: Spontaneous emission spectrum of optically pumped v3 VCSELs for 5, 7 and 13 μm mode sizes at input pump power of 30 mW. The coupling losses have not been compensated. 50X objective is used.

7.6.3 Discussion

Most of the uncertainties that were observed with previous version, such as issues with DBR deposition and etch-back of the epitaxy, have been eliminated with fabrication of v3 version of VCSELs. However, the bonding results were even worse.

The resonance of spontaneous emission with optical pumping is observed again, but the lasing condition has not been reached. The wavelength at which the resonance occurs is again significantly shifted from targeted lasing wavelength. One possible reason for this can be the deviation of the thicknesses of epitaxial layers. The epitaxial layers grown on a 2-inch wafer would have relatively uniform thickness only in the central part of the wafer. The samples used in this fabrication come from the parts of the wafer closer to the edge. Therefore, it can be assumed that layer thicknesses may not match the previously measured values.

With no remaining TJ2 epitaxy samples, it was not possible to re-optimize the device design and attempt another fabrication in effort to demonstrate lasing.

7.7 v4 VCSEL results and discussion

The new epitaxy was obtained for final fabrication attempt, aiming at static demonstration of the lasing only. Some of the features introduced for high-speed design, such as short cavity and TJ, have been dropped and the PIN epitaxy is designed as given in Table 4.6 in chapter 4. The thicker contact layers reduce the possibility of issues with formation of contacts and reduce the risk of over-etching during second mesa dry etching step. The implant apertures have not been fabricated once again. To compensate, the low doped current blocking layers are introduced to help with lateral current spreading.

7.7.1 Fabrication results

The investigation of a cross-section of the epitaxy using SEM showed excellent agreement of layer thicknesses with the design. Therefore, no adjustments of epitaxy or additional phase matching layers were needed. The v4 design was fabricated as described in 4.

The bonding of pin epitaxy samples gave excellent results. Several samples were bonded, all successfully with only negligible detached areas due to some defects on the sample surfaces, as shown on Fig. 7.31. Due to time constrains only one sample with v4 design was fully fabricated.

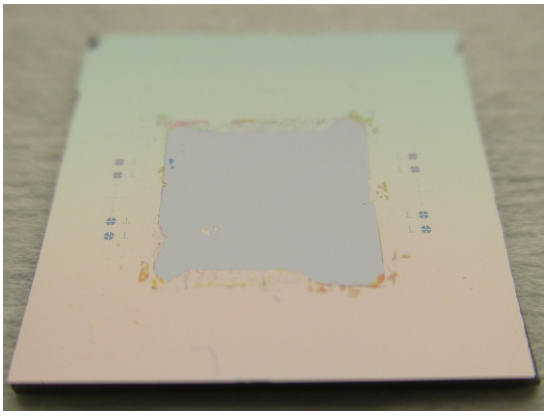


Figure 7.31: Photograph of the bonded sample for v4 VCSEL.

Thanks to good bonding result and uniform III-V film, the rest of the fabrication went mostly as expected. The changes in the fabrication procedure for v4 VCSELs were discussed in previous chapter. The partial selective removal of top InGaAs contact layer and splitting of fabrication of ohmic contacts for *n*- and *p*-type has been described. The microscope image of the device with completed etching and both ohmic contacts is shown on Fig. 7.32. The difference in color between InGaAs and InP, as well as between annealed and non-annealed contacts, is noticeable.

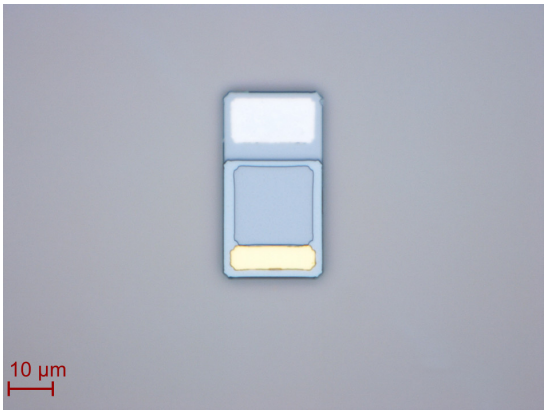
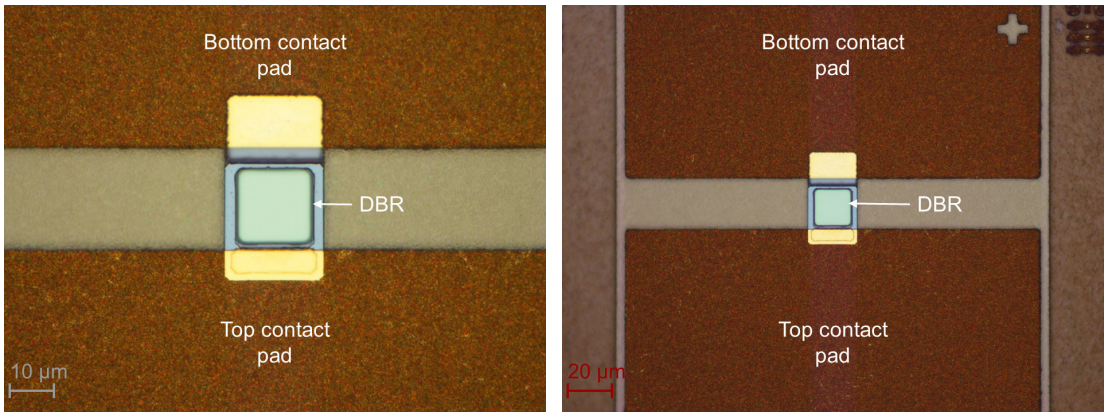


Figure 7.32: Microscope image of the v4 VCSEL with formed mesa and both ohmic contacts.

Some difficulty was encountered with the BCB etch-back process after planarization. The etch rate was significantly slower than previously measured. This is most likely caused by the different conditions in the chamber before the etch. As a result, the etched BCB surface was left rough, in similar way as with one v3 sample. This didn't cause any noticeable issues with adhesion of deposited contact pads, as metallization and lift-off gave good results. Another concern was the increased step height difference from BCB to contact layers (around 420 nm), due to larger height

difference of two contact layers, which may cause metal disconnect. The inspection with optical microscope has shown no evidence of this, however it can only be confirmed during characterization.

The fully fabricated v4 VCSELs are shown on Fig. 7.33. The rougher surface of the BCB causes darker color of the metal that is deposited on it, while the metal deposited on the device itself shows typical smooth gold color.

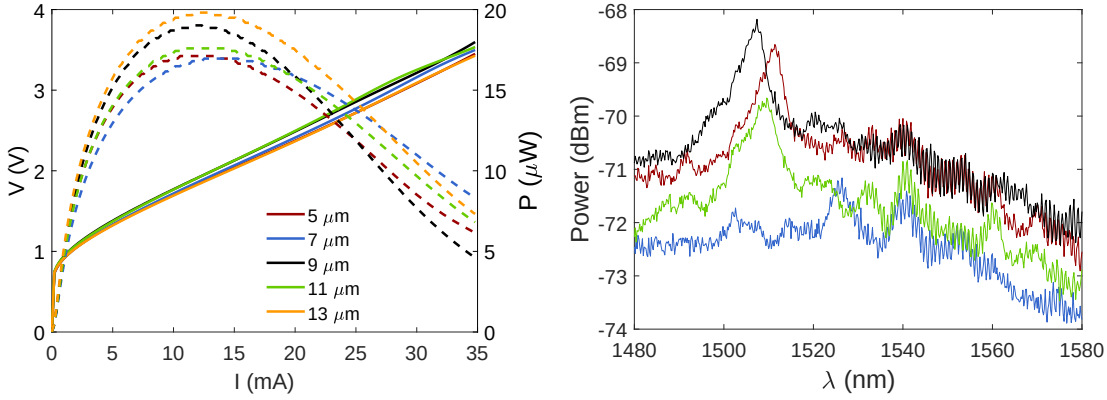


(a) **(b)**

Figure 7.33: Microscope images of the v4 VCSELs after finished fabrication.

7.7.2 Characterization results

The characterization of v4 VCSELs with electrical pumping showed only spontaneous emission, similar to previous versions. The Fig. 7.34a shows results for some of the brightest VCSELs with aperture sizes of 5–13 μm. The V-I characteristics are similar, with differential resistance around 70 Ω and turn-on voltage around 0.73 V. The emitted optical power is captured with 50X objective this time, which has 3 dB higher loss at 1.55 μm wavelength. To compensate, the entire output is directly connected to the photodiode without 3-dB splitter. The measured output power is over three times higher than for v2 VCSELs. The spectrum is captured for several devices at peak



(a) **(b)**

Figure 7.34: (a) Voltage-power-current characteristics of v4 VCSELs for 5, 7, 9, 11 and 13 μm mode size. The solid lines show voltage versus current and dashed lines show corresponding optical power. (b) The emission spectrum of v4 VCSELs under electrical pumping with current for maximum output. The coupling losses have not been compensated. 50X objective is used.

output power by coupling total output into the OSA. The Fig. 7.34b shows some of the typical spectrums, which look similar for devices of all sizes. The multiple peaks of ASE are noticeable, with strongest ones around 1510 nm and 1540 nm.

An example of NIR camera images of electrically pumped spontaneous emission from largest v4 VCSEL and LED are shown on Fig. 7.35. The emission is strongest near the top contact and gradually reduces going towards the opposite side of the air-post mesa, which gives evidence of the current diffusion in absence of the aperture.

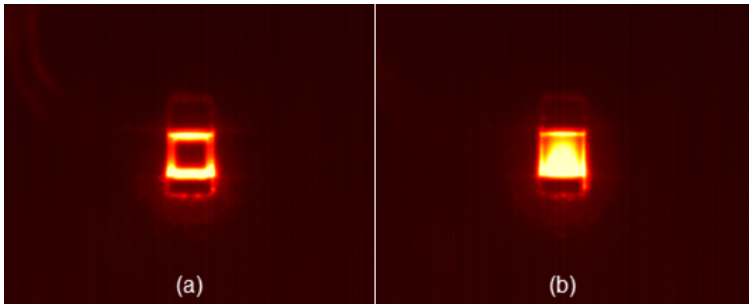


Figure 7.35: NIR camera images of electrically pumped spontaneous emission of v4 (a) VCSEL and (b) LED for mode size of 13 μm at current for maximum output. Seen with 50X objective.

Optical pumping of the v4 again only showed spontaneous emission. The Fig. 7.36 shows NIR camera images of long-wavelength spontaneous emission under pulsed optical pumping with input power of 30 mW. The light emission is observed only around the DBR and scattered on the mesa edges, the same as with electrical pumping but more uniform as the center of the device is pumped directly.

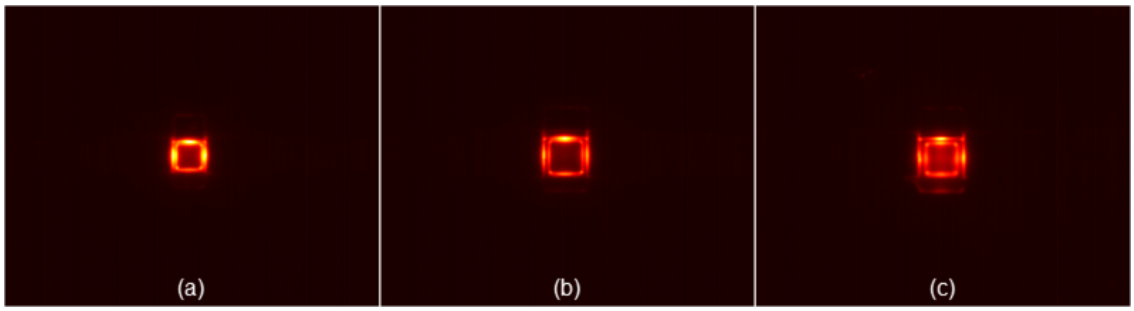


Figure 7.36: NIR camera images of optically pumped spontaneous emission of v4 VCSELs with mode sizes of 13 μm for input pump power of 30 mW. (a) The narrower compact design introduced with v3. (b) The wider v2 design. (c) An example with modified DBR and stronger emission from the center. Seen with 50X objective.

Optical spectrum of emission under optical pumping with input power of 30 mW was captured with OSA using single mode fiber. The Fig. 7.37 shows spectrum of several typical VCSELs. The overall power level is lower and signal is noisier due to use of single mode fiber. The ASE peak is observed in spectrum of most of the devices. It is more prominent for larger devices and with narrower design, as the pump spot is overlapping more with DBR. For smaller devices or devices with wider design, the pump spot overlaps relatively more with III-V around the DBR and broad spontaneous emission is more dominant. There are two groups of ASE peaks that appear in spectrum of various devices: one group is in range of 1500-1510 nm and second around 1520 nm. Which peak group will be observed for any laser has no correlation with any variations in the design. The variation in exact wavelength shows some correlation with grating design, with larger

grating bar widths shifting peak to higher wavelengths. The peaks that appear in first group are always stronger.

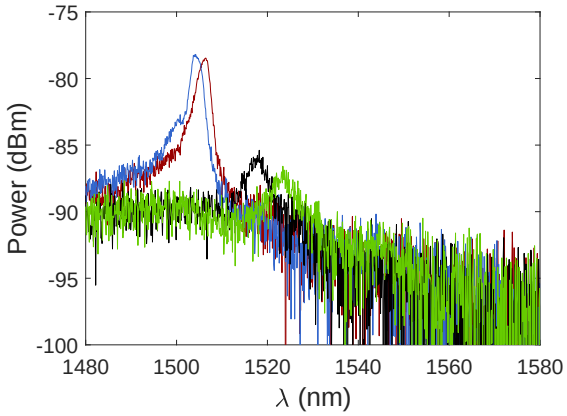


Figure 7.37: Spontaneous emission spectrum of several optically pumped v4 VCSELs for mode size of 13 μm for input pump power of 30 mW. SMF is used and the coupling losses have not been compensated. 50X objective is used.

Since the resonance peak seem to be shifted form the target wavelength, an attempt has been made to modify the structure and shift the wavelength by 20–30 nm. This was done by removing the DBR, depositing additional phase shift layers of 10 nm SiO_2 and 20 nm of a-Si and finally redepositing and patterning the DBR layers. The Fig. 7.38a shows the original DBR reflectivity spectrum (simulated from design and measured), and the Fig. 7.38b shows the comparison with modified DBR with phase control layers. The reflectivity at pump laser wavelength at 980 nm is slightly increased.

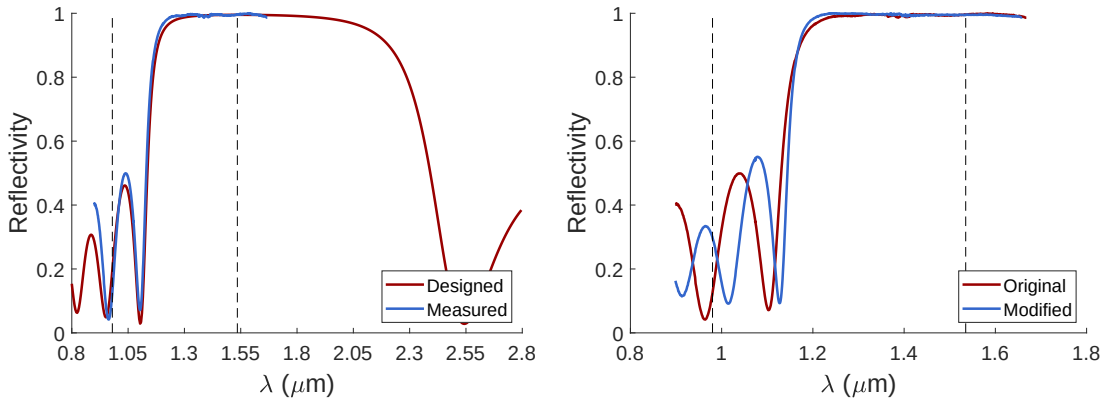


Figure 7.38: (a) The plot of measured and simulated reflectivity spectrum of the originally deposited DBR. (b) The comparison of original and modified DBR.

Unfortunately, during processing for new DBR, the metal contact pads detached from the BCB surface. Therefore, it was not possible to repeat the characterization with electrical pumping. The characterization with optical pumping was done, but still no lasing was observed. The strong ASE peaks are observed again and, as intended, they have been shifted for about 20 nm. The Fig. 7.39a shows several typical spectrums with peaks in range from 1525 nm to 1545 nm. The one device showed particularly strong peak 1545 nm, which is shown for varying pumping power levels on the

Fig. 7.39b. The peak intensity rises with increasing pumping power, but saturates due to thermal roll-over. The NIR camera image of emission from this device is shown on third image on the Fig. 7.36. The increased light emission from the center of the DBR is noticeable.

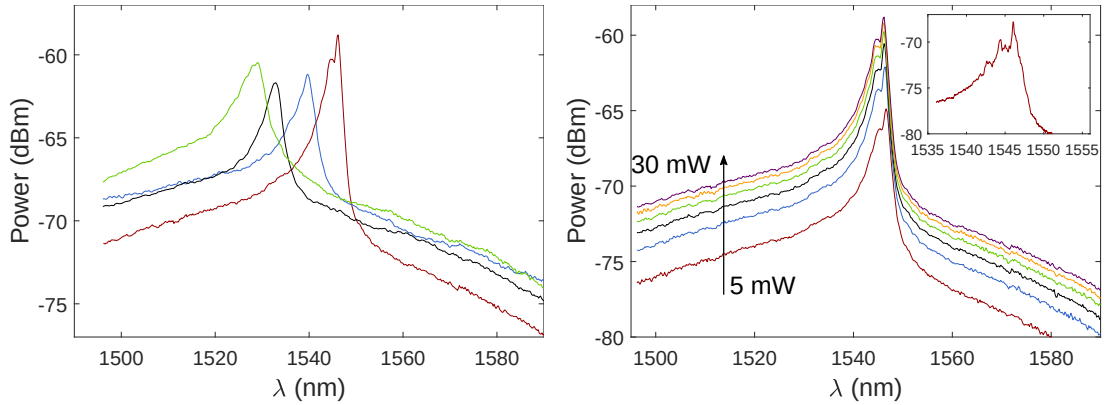


Figure 7.39: (a) Spontaneous emission spectrum of several optically pumped V4 VCSELs for mode size of 13 μm with modified cavity for input pump power of 30 mW. (b) The strongest ASE peak at varying input pump power in range 5–30 mW. The inset shows higher resolution measurement with multiple sub-peaks. MMF is used and the coupling losses have not been compensated. 50X objective is used.

7.7.3 Discussion

The fabrication of V4 was significantly improved over previous attempts with TJ2 epitaxy. The smooth surface of the PIN epitaxy enabled the excellent bonding result. After mesa etching the III-V, the bonding layer looks smooth and uniform in color. The partial removal of InGaAs contact layer was improvised using lithography mask for DBR but with negative tone photoresist, as the dedicated mask for this process was not designed and obtained. Therefore, the remaining narrow InGaAs parts that remained surrounding the central opening could have influenced the current injection. This would be avoided in future with dedicated mask design for this process.

The devices across the sample show consistent and uniform electrical and optical properties. No lasing is achieved but intensity of generated spontaneous emission is increased, showing that PIN epitaxy has highest gain of all that were tested. Amplified spontaneous emission is observed again, with multiple peaks showing in the spectrum and more pronounced than ever before.

The current diffusion was facilitated by the current blocking layer, and it is evident from the profile of the emission seen from the LED devices. However, in order to achieve a reasonably low threshold some form of current aperture needs to be employed.

The shift in the resonance wavelength is observed again, although it is significantly less than previously seen. The cause cannot be identified with certainty, and can only be attributed to random fabrication tolerance. The method of adjusting the resonance wavelength by reprocessing the sample and adding phase control layers has been proven successful. With added phase control layers, the emission is improved a stronger ASE is observed. However, the pumping efficiency is reduced due to higher reflectivity of the modified DBR at the pump wavelength ($\approx 30\%$).

One of the potential drawback of the V4 design is that the low-refractive-index layer in this design is only 160 nm thick. In chapter 4, the reflectivity of the HCG design was calculated to be higher than 99.99%. However, this was based on simple numerical simulation of the infinite grating. As was mentioned in chapter 2, the finite size gratings will have reduced reflectivity [139]. Together

with reduced low-refractive-index layer thickness and fabrication tolerances, the reflectivity of the HCG may not be sufficiently high and threshold would be increased.

7.8 Summary and discussion

This chapter summarizes the results of the experimental investigation of the VCSELs that was done over the duration of this project. The four different versions of the proposed design have been fabricated and tested using electrical and optical pumping methods.

The first version, V1, used relatively smooth epitaxy with tunnel junction, TJ1. Several samples were fabricated and characterized, but none of them showed lasing. The spontaneous emission was observed, but only from the aperture area even in case of optical pumping. This proved that implantation induced damages in the active region are not annealed during processing. However, the main issue was almost complete lack of emission under electrical pumping. To investigate, a most simple LED design was fabricated from the same epitaxy. Again, no light emission was observed under electrical pumping. The same devices were fabricated from other TJ epitaxy (TJ2) and tested also. In this case, LEDs showed proper light emission. Therefore, the TJ2 was used for next fabrication.

The poor surface morphology of TJ2 epitaxy led to low bonding yield and difficult fabrication. The two versions, with (V2) and without (V3) implant apertures, have been fabricated and tested. No lasing was reached by any of the V2 and V3 devices that were tested. However, strong spontaneous emission was observed with both electrical and optical pumping. Weak resonances have been observed in the spectrum of the spontaneous emission, but due to differences in epitaxial layer thicknesses and non-uniform bonding layers, these peaks were significantly shifted from targeted wavelength for this design.

The latest epitaxy was designed for easier and more reliable fabrication, with PIN structure. With excellent surface quality, the bonding of this epitaxy and fabrication of V4 VCSELs was very successful. No lasing was observed once more, but overall output power is improved and stronger ASE peaks are noted in the spectrum. The peaks were somewhat shifted, but the shift was compensated by reprocessing the sample to include additional phase control layers in the DBR mirror. The strong ASE peaks at target wavelength have been observed, but the lasing threshold was still too high.

The high doping levels needed for realization of tunnel junction, seem to lead to increased surface morphology which has direct impact on quality of wafer bonding. While this can be compensated to some degree by using the adhesive BCB bonding, the thin BCB layer is necessary for this design and it cannot help enough with extremely rough wafers as was TJ2. If the TJ is to be included in future work, the epitaxy quality needs to be at least as good as was observed for TJ1.

The lack of lasing is disappointing, but numerous issues have been handled in this pioneering work and with each version the results improved. The last obtained results showed good promise and it is believed that lasing is within reach.

One property that hasn't been much discussed much so far is the heat dissipation in this design. Some numerical simulations have been done and two weak points of this design are identified: the small mesa size and dielectric layer between III-V and Si. The small mesa means that all the generated heat is contained in small volume and cannot spread out in lateral direction. The contact pads are placed on BCB layer which has very low thermal conductivity, so heat transfer from metal pads towards the substrate is negligible and contact pads do not act as good heat sink. The need for vertical emission means that no heatsink can be fabricated on top of the DBR, and small margins do not leave enough space to place the heat sink around the DBR. Therefore, the main heat dissipation path is identified to be downwards trough the grating into the Si layer. However, this path is slowed down by the dielectric layers (SiO_2 and BCB) that exist between III-V and Si. In design with air-gap instead of SiO_2, the III-V would be bonded directly onto Si, and then air-gap would be formed only above the grating by selective wet etching. Therefore, the III-V would be still in contact in area outside the grating. The heat can travel laterally in III-V

above the grating and then downwards towards the Si next to the air-gap. Both designs have a trade-off and may give similar performance.

The possibly poor heat dissipation in the investigated design could be another leading cause for lack of lasing. This requires further research, especially when targeting the CW emission.

CHAPTER 8

Conclusion and Outlook

8.1 Summary and conclusion

This project aimed at demonstrating the novel electrically pumped hybrid VCSELs and investigating their high-speed operation. In this thesis, the design of the proposed laser is explained and experimental efforts to demonstrate it are presented.

The hybrid approach, by integrating III-V on silicon platform, opens the door to broader range of applications, and it is one of the main points that shaped and defined the proposed design. The key innovation in this design is the HCG which is used as one of the mirrors to form the cavity. While VCSELs with HCG have been demonstrated previously, here it is used specifically to optimize the laser for high-speed operation. The hybrid structure offers a high refractive-index contrast, so by defining the grating on the Si platform and employing the design for TM polarization, with shorter evanescent field penetration, a very compact bottom mirror for vertical cavity can be formed. Together with dielectric DBR as top mirror, the effective cavity length can be minimized. This is the key mechanism for reducing the photon lifetime which in turn leads to increased intrinsic modulation bandwidth.

The challenge in this work was adapting this design for electrical pumping while preserving the excellent performance that intrinsic design offers. The strategies for minimizing the parasitic elements have been considered. The tunnel junction approach for minimizing the series resistance of the device is adopted. The methods for current confinement are reviewed and two most applicable methods, implant and undercut apertures, have been investigated. The undercut apertures have been tested, but it was concluded that it cannot be used in most efficient way with epitaxial design that was available and their fabrication proved unreproducible. The implantation of protons has been extensively studied, tested and implemented in final designs. The ohmic contacts had to be optimized to prevent the deep metal spiking which would destroy the thin contact layers of the short cavity. The low-Au metallization approach is implemented and sufficiently low specific contact resistance has been demonstrated experimentally.

The wafer bonding is the key enabling fabrication technology used in this work, used to integrate the III-V onto SOI. It is the most critical process which directly determines the yield and influences the properties of the finished devices. The high roughness of the epitaxial wafers made it impossible to utilize the already established direct wafer bonding procedure. So alternative method need to be developed. The adhesive bonding method offers less strict requirements for surface morphology. The bonding using BCB polymer as the adhesive layer was investigated, focusing on the bonding with ultra-thin layers that are necessary due to the nature of the design. After long testing, plagued by limitations from the bonding tools available in the cleanroom, the stable and reliable procedure for bonding was implemented and optimized.

The complete process flow for fabricating the proposed lasers has been developed with CMOS-compatibility in mind. The fabrication is complicated and requires use of broad range of tools and processes, but generally it relies on well established procedures that are realiable and can be implemented easily for production on larger scale. The fabrication of several samples constituted

the largest portion of time spent on this project.

Four different versions of VCSELs have been fabricated and tested. The first version featured symmetrical mesa design with ring contacts surrounding the top mirror and air-post mesa. The proton implantation is employed to realize the current aperture. Due to issue with epitaxial design, the lasers showed no light emission under electrical pumping. The second version featured an asymmetrical mesa design with parallel contacts. It was made using a different epitaxy and implantation was done again for current confinement. However, due to the poor surface quality of this epitaxy, the bonding had low yield and non-uniformity of bonding layer was observed. Only spontaneous emission is observed with both electrical and optical pumping. However, the peaks of amplified spontaneous emission are observed in the spectrum and they suggest that cavity resonance was not matching the design. Furthermore, it was observed that active region remains damaged by the implantation process, as the light emission under optical pumping was observed only from non-implanted regions. In order to investigate the influence of the damaged active region, the fabrication of next version is done without the implant aperture. The bonding results were poor yet again and results were no better than with previous version. The optical pumping showed somewhat more prominent ASE peaks in the spectrum of spontaneous emission. The final version used a different epitaxy, without tunnel junction and with thicker contact layers. This version showed improved electrical properties and stronger spontaneous emission, but still no lasing is achieved. The resonance peaks are again observed but they occurred at wavelengths that were 20–30 nm shorter from target wavelength. The devices were modified by adding additional phase control layers to shift the resonance 20 nm forward. Very prominent ASE peaks are observed yet again, but still the threshold for lasing is not reached.

The research conducted in this project aimed at demonstrating the electrically pumped VCSELs. While lasing has not been achieved, the groundwork has been done by investigating the necessary components for electrical pumping and establish the overall design. The most time consuming task of developing and optimizing the complete fabrication procedure has been done, including the reliable wafer bonding method that is critical for this design.

8.2 Outlook and future work

The successful demonstration of lasing is close. Based on research presented in this thesis, the future investigation will go significantly quicker.

The issue of surface quality that occurred with epitaxies that contained highly doped TJ layers needs to be addressed. From example of TJ1 epitaxy, it is evident that sufficient smoothness is achievable and BCB bonding method can be successful. The performance of the tunnel junction should be improved at the same time. The series resistance of the VCSELs that were fabricated from TJ2 epitaxy was higher than even PIN devices. The optimization of TJ and contacts for achieving the ideal 50 Ω resistance should be achievable.

The current confinement remains one of the biggest obstacles. The proton implantation has shown that it can be used to direct the current, but it also leaves damages in the active region which may degrade the properties of the device. Redesigning the epitaxy to insert larger spacing between targeted layer for implantation and the active layers may be necessary. However, it may be limited by the short cavity design. The initial study of implantation in this work was influenced by the issues with ohmic contacts. Therefore, a more systematic study of implant apertures should be conducted, for both electrical and optical properties, if this method is to be used in future design. As an alternative, the undercut etching can provide more reliable performance and has advantage of ensuring optical guiding at the same time. Designing the epitaxy to achieve selective etching of only TJ layers, without affecting the active layer, should offer the best performance and it should be achievable.

The thermal properties of the design need to be further investigated. The design inherently has disadvantage in this regard. Fabricating the heatsink on top mirror side is not possible, as the output light is collected for that side. The hybrid design prevents creation of the heatsink below the structure, and the thick dielectric layer between heat source (active region of III-V) and

substrate slows down the heat flow towards the substrate. The most promising solution can be fabrication of the thick metal heatsink that would connect the top of the mesa and the Si substrate of the SOI directly. Alternatively, materials with better thermal conductivity, such as Al_2O_3, could be used between III-V and SOI to improve the heat flow towards the substrate.

Finally, after the successful lasing is demonstrated, the static and dynamic properties of the devices should be investigated. The threshold current is critical parameter for the targeted application as it influences the efficiency of the laser. The modal properties of the lasing spectrum should be studied. The heterograting design should ensure mode confinement, but larger devices may still suffer from higher transverse mode emission. Smaller devices should be able to reach single mode emission but at the price of lower output power. Additional methods for suppression of higher modes may be necessary. The dynamic characterization should provide information on intrinsic and parasitic response of the lasers. The intrinsic speed is expected to reach, and probably surpass, the state-of-the-art reported values. The main concern is minimizing the parasitic influence so that this potential can be exploited.

In this work, the vertical emission was pursued. However, the HCG enables the possibility of coupling the light into in-plane direction. The emission into the silicon waveguide from VCLs with similar design as investigated here was demonstrated previously in our group with optical pumping [64]. The adapting of the design suggested in this work for lateral emission would be trivial, with no issues for the fabrication. The lateral emission would allow for hybrid top mirrors with metal covering the short dielectric DBR and acting as an efficient heatsink.

Alternative designs based on the same hybrid platform can also be pursued. It was discussed shortly in chapter 2 about the possibility of designing the HCG to act as an ultrahigh-Q resonator. By fabricating the grating into the III-V epitaxy with active layers, such HCG resonator can work as a laser [224]. Such lasers have been studied in our group recently also. The HCG-resonator laser is realized as sub-micron thick III-V grating bonded to the box layer of the SOI. The devices showed very high 3-dB bandwidth under optical pumping. It is planned to adapt the design for electrical pumping in the future.

A new type of grating reflector, named hybrid grating (HG), has been reported [225, 226]. The HG is realized by directly bonding the high-refractive-index III–V material on a Si grating. The III–V layer has thickness comparable to the grating layer, and introduces more guided mode resonances which lead to significantly wider high-reflection bandwidth compared to the HCG reflectors. By using the active III-V layer and fabricating the second mirror on top, a vertical cavity laser can be formed. This structure would be similar to the design investigated in this work, but without the thick dielectric layer between the III-V and Si. This could lead to even more compact structure with higher intrinsic speed, but the main advantage would be better heat dissipation towards the substrate. While direct wafer bonding is preferred for realizing hybrid structure, the ultrathin BCB bonding developed for this work could be used without degrading the HG properties. Alternatively, just like with HCG, the HG can also work as a standalone high-Q resonator without the need for second mirror [227]. The lasers based on this design have also been recently demonstrated with optical pumping by our group with promise of high bandwidth.

It can be concluded that the work done during this Ph.D. project and presented in this thesis provides a groundwork for entire platform of hybrid III-V-on-Si VCL with grating mirrors. Whether they use HCG or HG structure, two-mirror cavity or high-Q resonator design, the electrical pumping approaches developed in this work would be applied in similar way. By employing the similar concepts as discussed in first part of this thesis, these hybrid lasers can exhibit the exceptionally high intrinsic modulation bandwidth. Considering the inherent high energy efficiency of the VCLs and possibility of designing the light output to be off-chip or in-plane, thanks to the gratings, these lasers could find application in wide range of optical interconnects, from micrometer length links in silicon photonics to long distance fiber links in mega data centers.

APPENDIX A

Fabrication process flow

This appendix lists all the steps in the process flow for fabrication of hybrid VCSELs investigated in this thesis. Almost all of the fabrication is done in state-of-the-art cleanroom facility at DTU Danchip using tools and facilities available during the time of this Ph.D. project, with the exception of proton implantation that was performed at the Ion Technology Center (ITC), Ångström Laboratory, Uppsala University. The recipes and processing times will be given as tested and used, but may not give the same result at later time due to changing conditions.

The fabrication of V2 version is given here. Some of the differences in fabrication of other versions has been outlined previously in chapters 6 and 7. The III-V epitaxy and SOI structure are repeated in Tables A.1 and A.2.

Table A.1: Structure of TJ2 III-V epitaxy.

Material	Thickness (nm)	Doping (cm^{-3})	Period	Function
InGaAs	20	undoped		Protective cap layer
InP	435	n-type (1.5×10^{18})		Bottom contact layer
InP	30	n-type (2×10^{19})		TJ (n^+)
InAlAs	30	p-type (2×10^{19})		TJ (p^+)
InAlAs	35	undoped		Cladding
InGaAlAs	7.5	undoped		Barrier (tensile strain)
InGaAlAs	6.5	undoped	7	Well (compressive strain)
InGaAlAs	7.5	undoped	7	Barrier (tensile strain)
InP	300	n-type (1.5×10^{18})		Top contact layer
InGaAs	190	undoped		Etch stop layer
InP	350 μm	n-type		Substrate

Table A.2: Structure of SOI wafer.

Material	Thickness (μm)	Function
Si	0.480	Device layer
SiO_2	1	BOX
Si	575	Substrate

1. SOI sample preparation (SOI wafer)

Cleaving	Cleave 2" SOI wafer into 1.5 cm × 1.5 cm square dies using tungsten tip. Wafer should be covered with photoresist to protect the surface from particles.
Solvent cleaning	Acetone – 5 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min in ultrasonic tub at high strength. Blow dry with N_2 gun.

2. E-beam lithography for bottom grating (SOI sample)

Resist coating	Spin-coat the sample with 1:1 diluted (5.5%) ZEP520A resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 60 s, 2000 rpm/s, 3000 rpm Expected resist thickness: 145 nm.
Softbake	Bake sample on hotplate at 160 °C for 2 min.
E-beam exposure	JEOL JBX-9500FS Dose 250 μC/cm^2, SHOT A,17, current 2 nA, aperture 4 (60 μm). Condition file '2na_ap4'. Chip cassette.
Development	Develop in ZED-N50 for 60 s. Agitate by hand. Rinse in IPA for 30 s. Blow dry.
Postbake	Bake sample on hotplate at 100 °C for 3 min.
Inspection	Check pattern using optical microscope. Check pattern using SEM.

3. Si dry etch (SOI sample)

Si etch	ASE, Bosch process: Pressure 10 mTorr, Temperature 10 °C, 12 etch/passivate cycles: Etch step: 50 sccm C_4F_8, 50 sccm SF_6, RF – 13.56 MHz, coil/platen power – 500 W/30 W, time – 5 s; Passivate step: 50 sccm C_4F_8, RF – 13.56 MHz, coil/platen power – 400 W/0 W, time – 3 s. Sample on 4" carrier Si wafer.
Resist removal	Dip in Microposit™ Remover 1165 for 3 min. Rinse in DIW. *This step should be done right before RCA-1 cleaning step.*

4. III-V sample preparation (III-V sample)

Cleaving	Cleave 2" III-V wafer into 7 mm × 7 mm square dies using tungsten tip. Wafer should be covered with photoresist to protect the surface from particles.

Solvent cleaning	Acetone – 5 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min in ultrasonic tub at high strength. Blow dry with N_2 gun.
Inspection	Check for particles and surface roughness using Nomarski microscope.
Cap layer removal	Wet etch of InGaAs in 1 H_2SO_4 (96%) : 8 H_2O_2 (31%) : 8 H_2O for 5 s. Rinse in running deionized (DI) water.
Cavity length adjustment	MORIE etch for InP in RIE. Precondition empty chamber. Etch for 1 cycle and 30 seconds. Preconditioning process: 10 sccm CH_4, 10 sccm H_2, pressure – 100 mTorr, RF power – 60 W, time – 10 min; Cyclic etch process: 4.2 sccm CH_4, 33.6 sccm H_2, pressure – 80 mTorr, RF power – 60 W, time – 2.5 min; Cyclic descum process: 50 sccm O_2, pressure – 150 mTorr, RF power – 60 s for 3 s then 20 W for 30 s. No carrier wafer.

5. RCA-1 cleaning (SOI sample)

Preparing the solution	1 N_4OH (95–97%) : 1 H_2O_2 (31%) : 5 H_2O (25 ml : 25 ml : 125 ml) Mix H_2O and NH_4OH and heat up until 70–80 °C. Add H_2O_2.
RCA-1 clean	Dip SOI sample into the solution. Keep at 70–80 °C for 10 min. Rinse with DI water. Blow dry with N_2
Inspection	Inspect for particles using optical microscope.

6. Dummy cavity layer deposition (III-V sample, test Si sample)

SiO_2 deposition	PECVD deposition of SiO_2. 1420 sccm N_20, 12 sccm SiH_4, 392 sccm N_2, pressure – 550 mTorr, temperature 300 °C, RF – 380 kHz, power – 60 W, time – 2:30 min. Target thickness 200 nm.
Thickness measurement	Measure oxide thickness on dummy Si sample using Ellipsometer.

7. Spin-coating BCB for bonding (III-V sample)

BCB spin-coating	Spin-coat the sample with 1:8 diluted Cyclotene 3022-35. 1. 5 s, 500 rpm/s, 500 rpm 2. 40 s, 1000 rpm/s, 3000 rpm No adhesion promoter.
Precuring	Bake sample on hotplate at 160 °C for 1 min.

8. Manual bonding (III-V sample, SOI sample)

Bond samples	Put the III-V sample upside down on the SOI. Gently apply pressure over the sample to improve bonding.

9. Mechanical bonding and BCB curing (Bonded sample)

High pressure bonding	Load sample into the NILT CPB. Pressure – 4 bar, Temperature profile: 10 °C/min to 150 °C; 10 min at 150 °C; 2 °C/min to 250 °C; 1.5 h at 250 °C; cool down to 50 °C.

10. Substrate removal (Bonded sample)

InP substrate etch	Wet etch in HCl (37%). Use continuous magnetic stirring. Approximately 1 hour. Rinse in running DI water. Blow dry with N_2 gun.
Resist spin-coating	Spin-coat the sample with AZ 5214E resist.
Softbake	Bake sample on hotplate at 90 °C for 90 s.
Cleaving of ridges	Gently cleave of ridges using tungsten tip.
Resist removal	Acetone – 5 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min. Blow dry with N_2 gun.

11. Deposition of hard mask layer for first mesa (Laser sample, test Si sample)

Si_3N_4 deposition	PECVD deposition of Si_3N_4. 40 sccm SiH4, 55 sccm NH3, 1960 sccm N2, pressure – 900 mTorr, RF – 13.56 MHz, power – 20 W, time – 19 min. Target thickness is 200 nm.
Thickness measurement	Measure nitride thickness on dummy Si sample using Ellipsometer.

12. Photolithography for first mesa (Laser sample)

Adhesion treatment	hexamethyldisilazane (HMDS) vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ 5214E resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 40 s, 2000 rpm/s, 4000 rpm Expected resist thickness: 1.5 μm.
Softbake	Bake sample on hotplate at 90 °C for 90 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 130 mJ/cm^2 (10 s at 13 mW/cm^2, changed to 11.5 s at 11 mW/cm^2). Vacuum contact.
Development	Develop in AZ 726 MIF developer for 60 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.

13. Hard mask dry etch for first mesa (Laser sample)

Hard mask etch	RIE nitride etch process. Use laser interferometer to stop etch. 1 sccm O_2, 15 sccm CHF_3, Pressure – 10 mTorr, RF power – 13 W, time – 10 min.
Resist removal	Acetone – 5 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min. Blow dry with N_2 gun.
Mask height measurement	Measure height of the hard mask layer using Dektak profilometer.

14. First mesa dry etch (Laser sample)

III-V dry etch	MORIE etch for InP in RIE. Precondition empty chamber. Etch for 12 cycles. Use laser interferometer to stop etch. No carrier wafer.
Mesa height measurement	Measure height of the mesa with mask layer using Dektak profilometer.

15. Mask for implantation (Laser sample)

Adhesion treatment	HMDS vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ 5214E resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 30 s, 1000 rpm/s, 1500 rpm Expected resist thickness: 2 μm.
Softbake	Bake sample on hotplate at 90 °C for 90 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 130 mJ/cm^2 (10 s at 13 mW/cm^2, changed to 11.5 s at 11 mW/cm^2). Vacuum contact.
Development	Develop in AZ 726 MIF developer for 60 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.
Hard mask etch	RIE nitride etch process. Time – 10 min. Use laser interferometer to stop etch.

16. Proton implantation (Laser sample)

Implantation	Ion species - proton H^+, dose – 1×10^{14} cm^2, energy – 100 keV, angle – 7°, temperature – room temperature.
Resist removal	Acetone – 20 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min. Blow dry with N_2 gun.
Descuming	Plasma asher. O_2 plasma, pressure – 0.2 mbar, power – 100%, time – 10 min.
Hard mask etch	RIE nitride etch process. Time – 10 min. Use laser interferometer to stop etch.

17. Deposition of hard mask layer for second mesa (Laser sample, test Si sample)

Si_3N_4 deposition	PECVD deposition of Si_3N_4. Time – 10 min. Target thickness is 100 nm.
Thickness measurement	Measure nitride thickness on dummy Si sample using Ellipsometer.

18. Photolithography for second mesa (Laser sample)

Adhesion treatment	HMDS vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ 5214E resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 40 s, 2000 rpm/s, 4000 rpm Expected resist thickness: 1.5 μm.
Softbake	Bake sample on hotplate at 90 °C for 90 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 130 mJ/cm^2 (10 s at 13 mW/cm^2, changed to 11.5 s at 11 mW/cm^2). Vacuum contact.
Development	Develop in AZ 726 MIF developer for 60 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.

19. Hard mask dry etch for second mesa (Laser sample)

Hard mask etch	RIE nitride etch process. Time – 5 min. Use laser interferometer to stop etch.
Resist removal	Acetone – 5 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min. Blow dry with N_2 gun.
Mask height measurement	Measure height of the hard mask layer using Dektak profilometer.

20. Second mesa etch (Laser sample)

III-V dry etch	MORIE etch. Precondition empty chamber. Etch for 10 cycles. Use laser interferometer to stop etch. No carrier wafer.
Mesa height measurement	Measure height of the mesa with mask layer using Dektak profilometer.
Damage wet etch	Wet etch of damaged surface in 1 HCl : 1 H_2O for 2 s. Rinse in running DI water. Blow dry with N_2 gun.
Mesa height measurement	Measure height of the mesa with mask layer using Dektak profilometer.
Hard mask etch	RIE nitride etch process. Time – 5 min. Use laser interferometer to stop etch.
Mesa height measurement	Measure height of the mesa with mask layer using Dektak profilometer.
Etch-stop layer removal	Wet etch of InGaAs in 1 H_2SO_4 : 8 H_2O_2 : 8 H_2O for 10 s. Rinse in running deionized (DI) water. Blow dry with N_2 gun.

21. Photolithography for thin ohmic contacts (Laser sample)

Adhesion treatment	HMDS vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ nLOF 2020 resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 30 s, 3000 rpm/s, 3800 rpm Expected resist thickness: 2 μm.
Softbake	Bake sample on hotplate at 110 °C for 60 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 115–118 mJ/cm^2 (9.1 s at 13 mW/cm^2, changed to 10.5 s at 11 mW/cm^2). Vacuum contact.
Postbake	Bake sample on hotplate at 110 °C for 60 s.
Development	Develop in AZ 726 MIF developer for 20 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.
Descum	Plasma asher. O_2 plasma, pressure – 0.2 mbar, power – 40%, time – 45 s.
Native oxide etch	Dip in buffered HF (BHF) for 1 min. Rinse in DI water. Blow dry with N_2 gun.

22. *n*-type metallization and lift-off (Laser sample)

Metal evaporation	E-beam evaporation of 30 nm Ni, 50 nm Ge and 20 nm Au
Lift-off	Acetone 10–20 min in ultrasonic tub at high strength, Ethanol 1 min, IPA 1 min. Blow dry with N_2 gun.
Inspection	Inspect contacts using optical microscope.
Alloying of ohmic contacts	RTA. 1 min at 150 °C and 15 s at 420 °C. Use graphite carrier.
Inspection	Inspect contacts using optical microscope.

23. Planarization (Laser sample, dummy 4" Si wafer)

Spin-coat adhesion promoter	Spin-coat sample with AP3000 adhesion promoter. 60 s, 2000 rpm/s, 2000 rpm.
Bake	Bake sample on hotplate at 150 °C for 1 min.
Spin-coat BCB	Spin-coat sample with Cyclotene 3022-46. 1. 5 s, 1000 rpm/s, 500 rpm 2. 40 s, 2000 rpm/s, 5000 rpm Expected resist thickness: 2.5 μm.
Precuring	Bake sample on hotplate at 150 °C for 2 min.

Thermal curing	Cure sample in oven with nitrogen atmosphere. 1. 5 min to 50 °C, 5 min at 50 °C 2. 15 min to 150 °C, 80 min at 150 °C 3. 60 min to 250 °C, 60 min at 250 °C 4. 15 min to 20 °C, 30 min at 20 °C Use carrier wafer for sample.

24. Etch-back of BCB (Laser sample, dummy 4" Si wafer)

BCB dry etch	RIE medium power BCB etch process. Use laser interferometer to stop etch when top of the III-V mesa is reached. 24 sccm O_2, 8 sccm CHF_3, pressure – 30 mTorr, RF power – 60 W for 10 s then 30 W, time – 10–13 min. Use dummy 4" Si wafer covered with BCB.
BCB height measurement	Measure the step height of the BCB relative to III-V mesa using Dektak profilometer.

25. Photolithography for opening III-V area (Laser sample)

Adhesion treatment	HMDS vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ 5214E resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 40 s, 2000 rpm/s, 4000 rpm Expected resist thickness: 1.5 μm.
Softbake	Bake sample on hotplate at 90 °C for 90 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 130 mJ/cm^2 (10 s at 13 mW/cm^2, changed to 11.5 s at 11 mW/cm^2). Vacuum contact.
Development	Develop in AZ 726 MIF developer for 60 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.

26. Opening III-V area (Laser sample, dummy 4" Si wafer)

BCB dry etch	RIE low power BCB etch process. Use laser interferometer to stop etch when bottom contact is reached. 12 sccm O_2, 3 sccm CHF_3, pressure – 30 mTorr, RF power – 60 W for 10 s then 10 W, time – 10–15 min. Use dummy 4" Si wafer covered with BCB.
Inspection	Check for remaining BCB on III-V using optical microscope.
Resist removal	Acetone – 5 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min. Blow dry with N_2 gun.
BCB height measurement	Measure the step height of the BCB realative to III-V mesa using Dektak profilometer.

27. Final etch-back of BCB (Laser sample, dummy 4" Si wafer)

BCB dry etch	RIE low power BCB etch process. 12 sccm O_2, 3 sccm CHF_3, pressure – 30 mTorr, RF power – 60 W for 10 s then 10 W, time – 3 min. Use dummy 4" Si wafer covered with BCB.
BCB height measurement	Measure the step height of the BCB realative to III-V mesa using Dektak profilometer.

28. Photolithography for contact pads (Laser sample)

Adhesion treatment	HMDS vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ nLOF 2020 resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 30 s, 3000 rpm/s, 3800 rpm Expected resist thickness: 2 μm.
Softbake	Bake sample on hotplate at 110 °C for 60 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 115–118 mJ/cm^2 (9.1 s at 13 mW/cm^2, changed to 10.5 s at 11 mW/cm^2). Vacuum contact.
Postbake	Bake sample on hotplate at 110 °C for 60 s.
Development	Develop in AZ 726 MIF developer for 20 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.
Descum	Plasma asher. O_2 plasma, pressure – 0.2 mbar, power – 40%, time – 45 s.

29. Thick-Au metallization and lift-off (Laser sample)

Metal evaporation	E-beam evaporation of 10 nm Ti, and 280 nm Au
Lift-off	Acetone 10–20 min in ultrasonic tub at high strength, Ethanol 1 min, IPA 1 min. Blow dry with N_2 gun.
Inspection	Inspect contacts using optical microscope.

30. Deposition of DBR (Laser sample, test Si sample)

SiO_2 and *a*-Si deposition	PECVD. SiO_2 should be predeposited in chamber. SiO_2 process: 1420 sccm N_20, 12 sccm SiH_4, 392 sccm N_2, pressure – 700 mTorr, temperature 300 °C, RF – 380 kHz, power – 150 W; *a*-Si process: 100 sccm SiH_4, pressure – 200 mTorr, temperature 300 °C, RF – 13.56 MHz, power – 10 W; 1. 7 s SiO_2 process for 10 nm; 2. 15.5 min *a*-Si process for 92.5 nm; 3. 2 min 43 s SiO_2 process for 265 nm; 4. 16.5 min *a*-Si process for 105 nm; Step 3. and 4. are repeated 3 times.

Thickness measurement	Measure each layer thickness on dummy Si sample using Ellipsometer.
DBR reflectivity measurement	Measure reflectivity spectrum using PL mapper.
DBR thickness measurement	Cleave the dummy sample and inspect layer thicknesses in SEM.

31. Photolithography for DBR etch (Laser sample)

Adhesion treatment	HMDS vapor priming in oven. Prebake for 5 min followed by HMDS prime for 5 min.
Resist coating	Spin-coat the sample with AZ 5214E resist. 1. 5 s, 1000 rpm/s, 500 rpm 2. 30 s, 2000 rpm/s, 1000 rpm Expected resist thickness: 2.3 μm.
Softbake	Bake sample on hotplate at 90 °C for 90 s.
Exposure	Exposure in mask aligner with 365 nm exposure wavelength. Exposure dose – 130 mJ/cm^2 (10 s at 13 mW/cm^2, changed to 11.5 s at 11 mW/cm^2). Vacuum contact.
Development	Develop in AZ 726 MIF developer for 60 s. Rinse in DI water. Blow dry with N_2 gun.
Inspection	Check development, alignment and pattern using optical microscope.

32. Etching of DBR (Laser sample)

DBR dry etch	RIE silicon dioxide etch process. Use laser interferometer to stop etch when III-V is reached. 2 sccm O_2, 16 sccm CHF_3, pressure – 100 mTorr, RF power – 60 W, time – 1 hour.
Inspection	Check for remaining DBR on III-V using optical microscope.
Resist removal	Acetone – 10 min, Ethanol – 1 min, Isopropanol (IPA) – 1 min. Blow dry with N_2 gun.
Descuming	Plasma asher. O_2 plasma, pressure – 0.2 mbar, power – 100%, time – 5 min.
DBR height measurement	Measure the step height of the DBR realative to III-V mesa using Dektak profilometer.

List of Acronyms

ASE . . . . . advanced silicon etcher

ASE . . . . . amplified spontaneous emission

BCB . . . . . benzocyclobutene

BOT . . . . . bandwidth over thickness

BOX . . . . . buried oxide

BTB . . . . . back-to-back

BTJ . . . . . buried tunnel junction

CMOS . . . . . complementary metal-oxide-semiconductor

CW . . . . . continuous-wave

DBR . . . . . distributed Bragg reflector

DFB . . . . . distributed feedback

DI . . . . . deionized

EMI . . . . . electromagnetic interference

FB . . . . . fractional bandwidth

FFE . . . . . feed forward equalization

FP . . . . . Fabry–Pérot

FWHM . . . . . full-width at half-maximum

GAN . . . . . global area network

GMR . . . . . guided-mode resonance

HCG . . . . . high-index-contrast grating

HDR . . . . . heat-to-data ratio

HMDS . . . . . hexamethyldisilazane

ICP . . . . . inductively coupled plasma

IR . . . . . infrared

IT . . . . . information technology

LAN . . . . . local area network

LED . . . . . light-emitting diode

MAN . . . . . metropolitan area network

MCEF . . . . . modulation current efficiency factor

MMF . . . . . multi-mode fiber

MORIE . . . . . metal organic reactive ion etching

NIR . . . . . near-infrared

NRZ . . . . . non-return-to-zero

OSA . . . . . optical spectrum analyzer

PECVD . . . . . plasma-enhanced chemical vapour deposition

PhC . . . . . photonic crystal

PL . . . . . photoluminescense

PR . . . . . photoresist

QD . . . . . quantum dot

QW . . . . . quantum well

RCWA . . . . . rigorous coupled-wave analysis

RIE . . . . . reactive ion etching

RTA . . . . . rapid thermal annealing

SEM . . . . . scaning electron microscope

SMF . . . . . single-mode fiber

SOI . . . . . silicon-on-insulator

TE . . . . . transverse electric

TJ . . . . . tunnel junction

TLM . . . . . transmission line method

TM . . . . . transverse magnetic

UV . . . . . ultraviolet

VCL . . . . . vertical-cavity laser

VCSEL . . . . . vertical-cavity surface-emitting laser

VNA . . . . . vector network analyser

VOA . . . . . variable optical attenuator

VOC . . . . . vertical outgassing channel

WAN . . . . . wide area network

WDM . . . . . wavelength division multiplexing

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